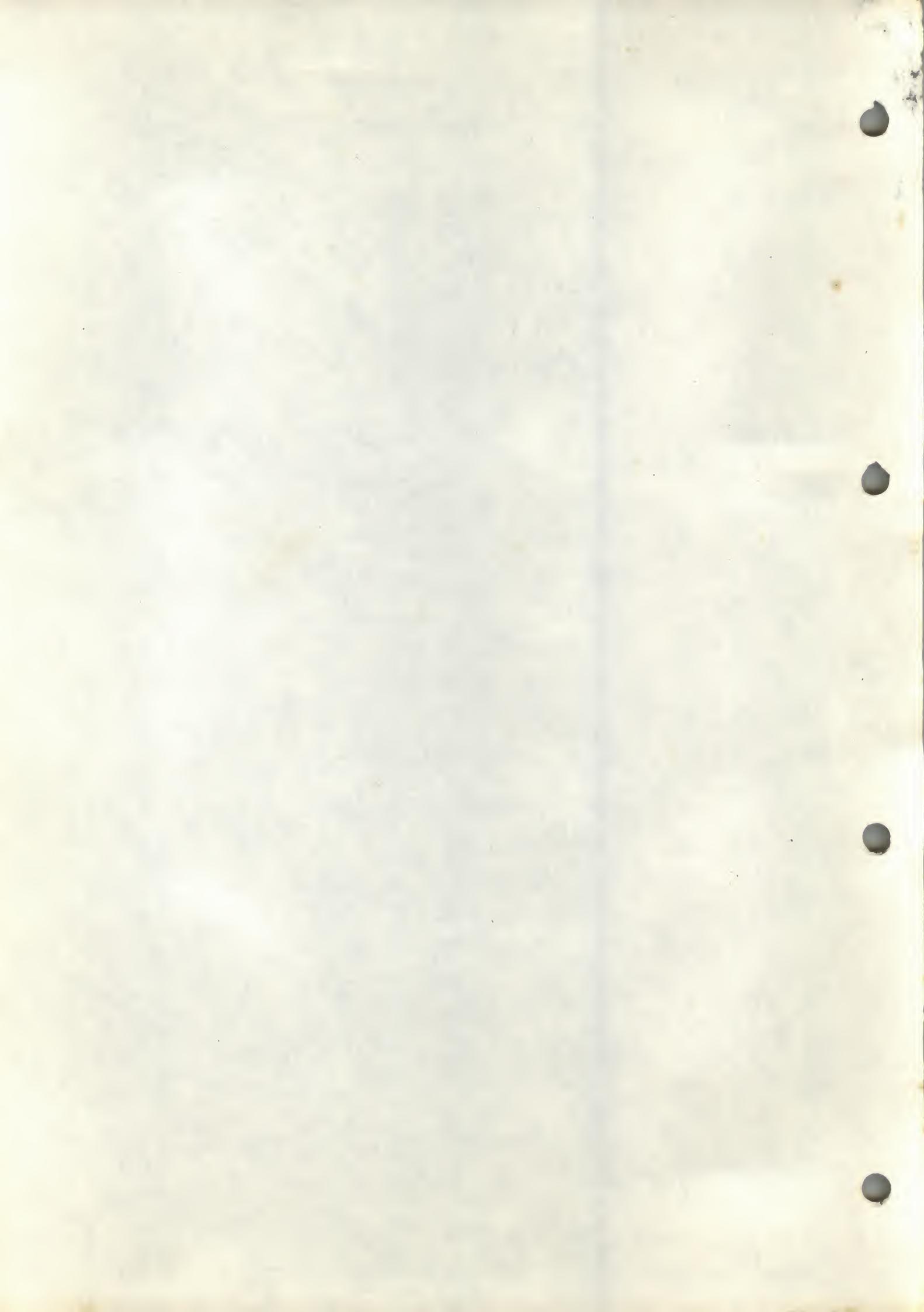
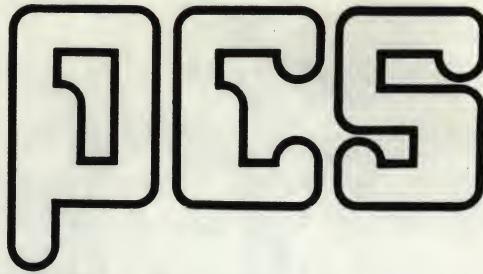


MULTI LINE UNIT

DLV 11 J

V 900.610





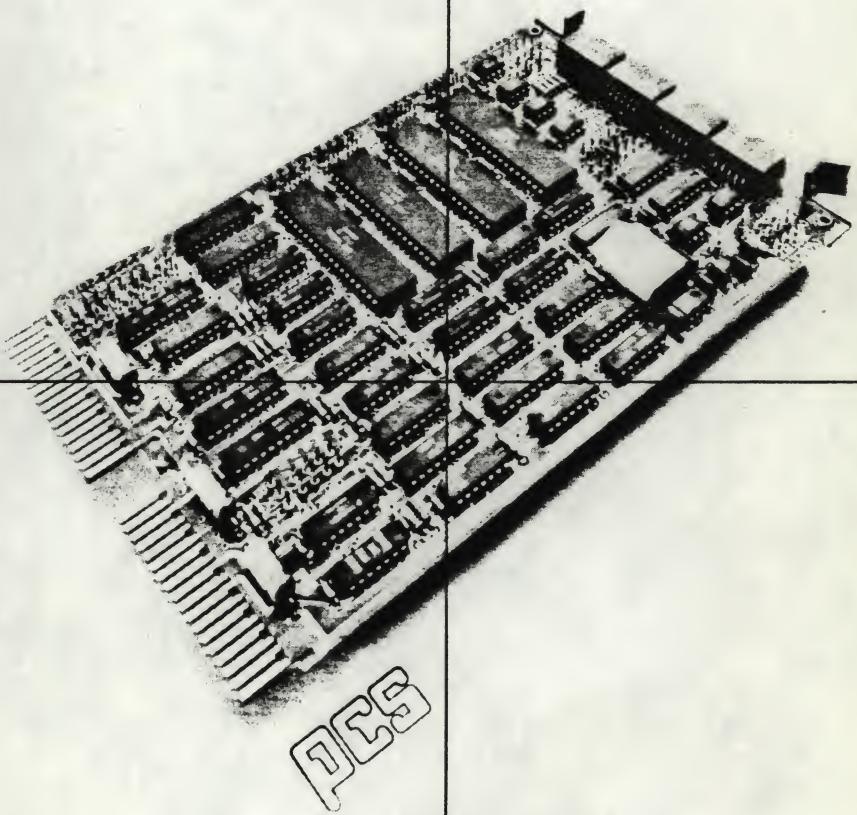
**Peripherie  
Computer Systeme GmbH**

# Vier-Kanal asynchrones, serielles-Interface

Die DLV 11-J dient als Interface zwischen 4 asynchronen, seriellen Kommunikationskanälen und dem Q-Bus im SII Rechner. Sie führt Seriell/Parallel- und Parallel/Seriell-Datenkonversionen mit je einem universellen asynchronen Empfänger/Sender (UART) pro Kanal durch. Der UART enthält alle Sender- und Empfängerfunktionen. Der Empfänger führt die Seriell/Parallel-Konversion von 7- oder 8-Bit-Codes durch, die Zeichen erscheinen im Datenpuffer rechtsbündig ohne Start-, Stop- und Paritätsbits. Der Sender führt die Parallel/Seriell-Konversion der Daten, die vom Q-Bus kommen aus und versieht diese mit Start-, Stop- und Paritätsbits. Die PCS 900610 enthält 16 Device-Register, die vom Programm individuell adressiert werden können.

Für jeden Kanal (0-3) gibt es die Empfangs-Kontroll/Status-Register (RCSR), Empfangsbuffer (RBUF), Sende-Kontroll/Status-Register (XCSR), Sendebuffer (XBUF)

**PCS 900.610**



#### **Technische Daten:**

- Vier unabhängige serielle Kanäle in einem Bus-Device
- Kompatibilität mit serieller EIA RS-232C und RS-423, AS 422 oder 20 mA Linienstrom (abhängig von Kanalkonfiguration und Kabelauswahl)
- Alle Kanäle können unabhängig voneinander konfiguriert werden:  
intern quarzgesteuerte Baud-Raten:  
150, 300, 600, 1200, 2400, 4800, 9600, 19200 oder 38400 Baud
- extern gesteuerte Baud-Rate

#### **Zeichenformate:**

- 7 oder 8 Datenbits, 1 oder 2 Stopbits, bei Bedarf Parität (ungerade oder gerade)
- Kanal 3 kann der Systemkonsole zugeordnet werden
- Bei Empfang eines „breaks“ auf Kanal 3 kann der Prozessor in den Halt-Mode gehen oder einen Bootstrap durchführen.
- Hard- und Software äquivalent zu vier PCS 900615.

Größe Dual Slot  
Stromversorgung + 5V / 1A  
+ 12V/0,25A  
normierte Busbelastung 1,0 AC, 1,0 DC

#### **Option**

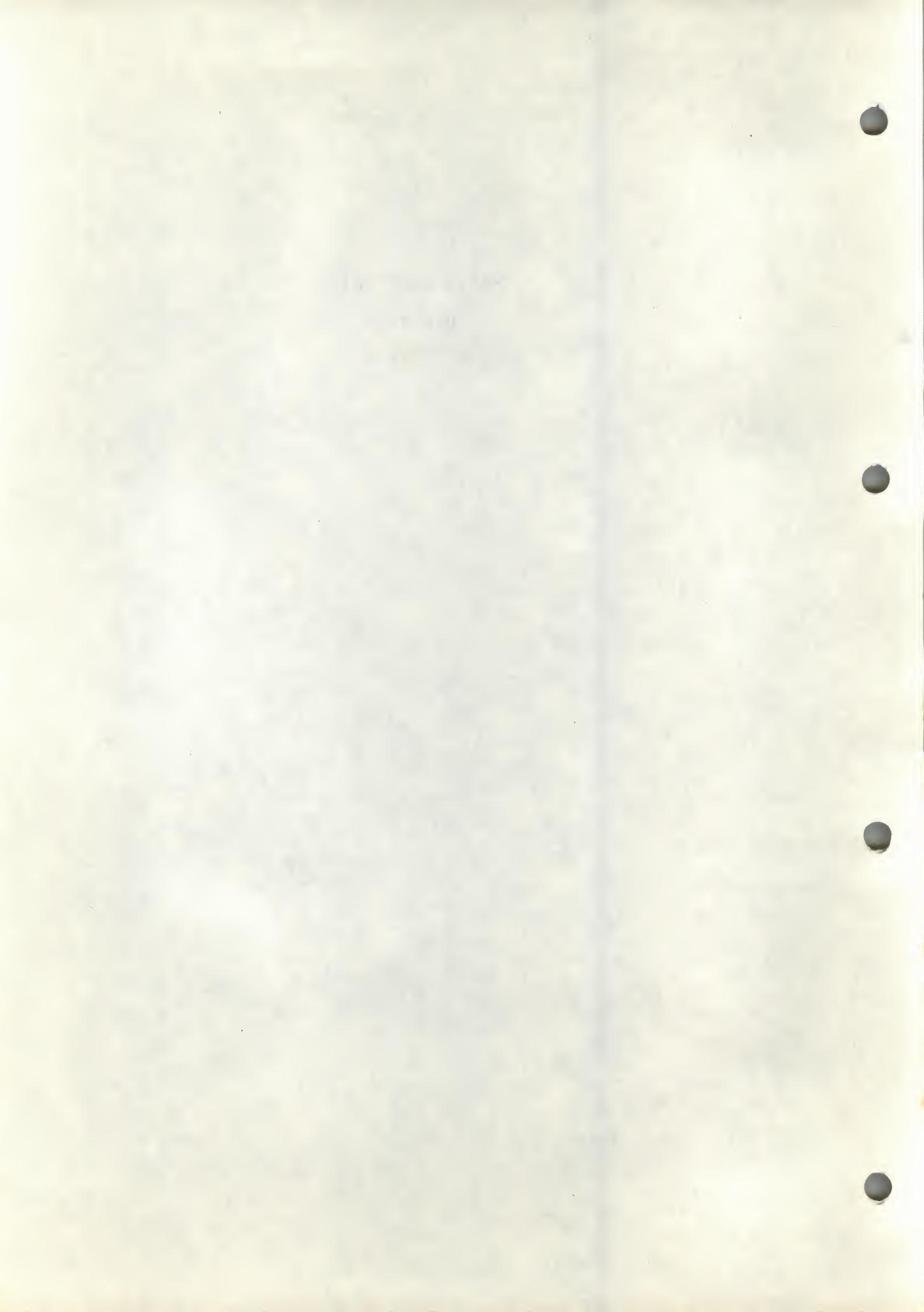
Liniенstrom-Pegelwandler für 4 Kanäle. Umsetzung von V24 auf 20mA Liniestrom (bis 9600 Baud)



MILTI LINE UNIT

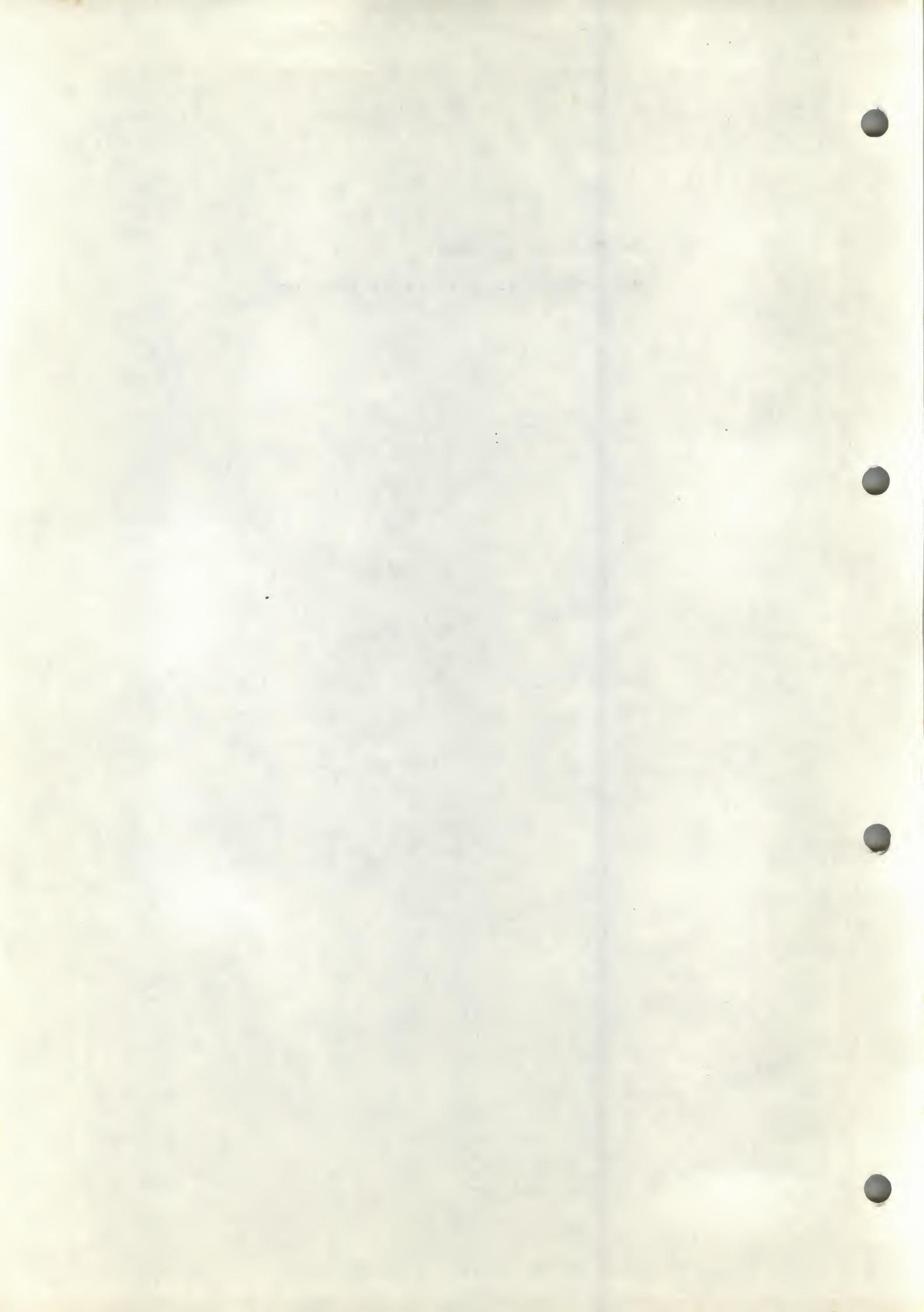
DLV 11 J

D 900.610



Beschreibung siehe:

Microcomputer Interfaces Handbook



DLV11-J

Four Asynchronous Serial Interfaces

900.610

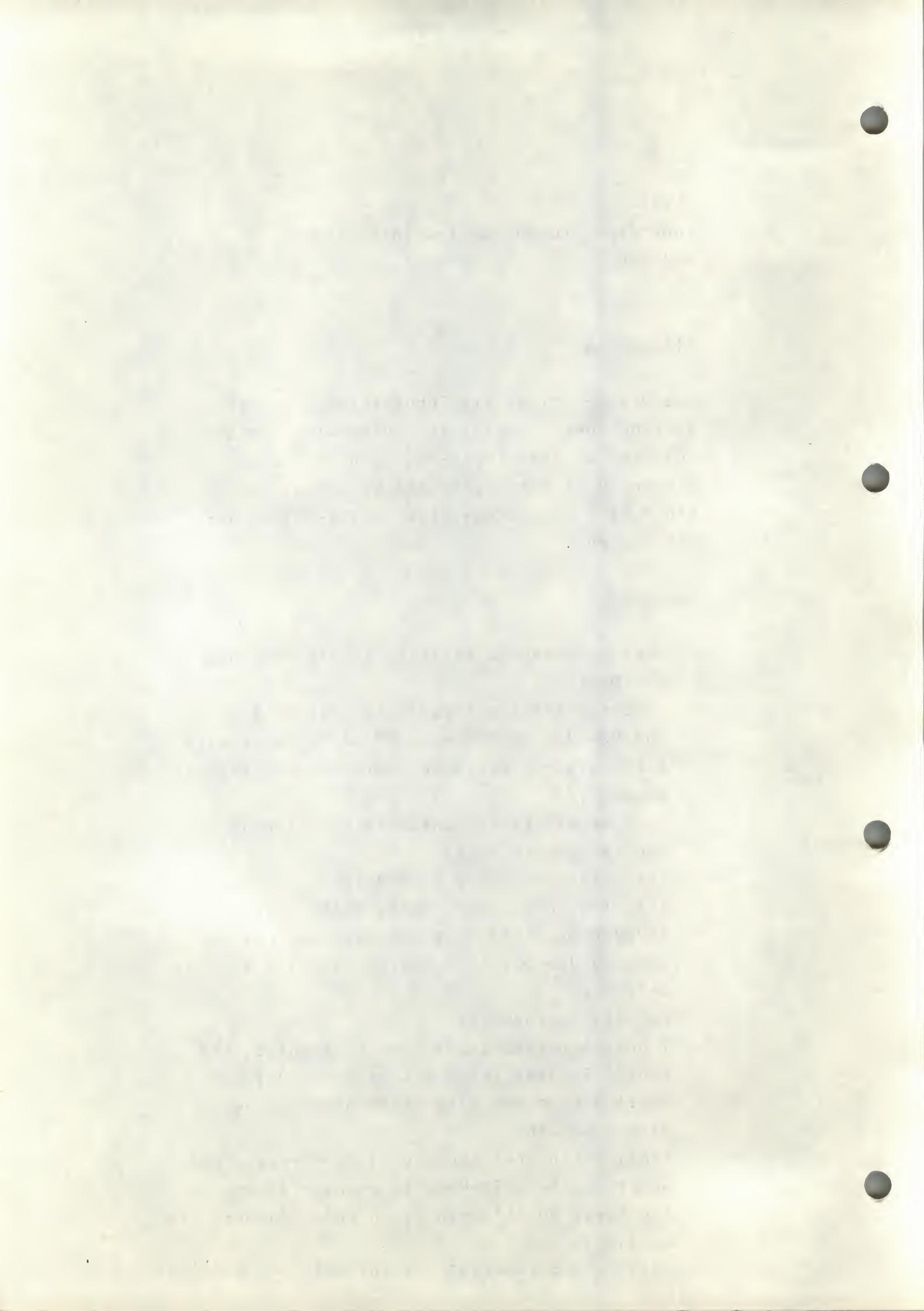
### Allgemeines

Die DLV11-J dient als Schnittstelle zwischen 4 asynchronen, seriellen I/O-Geräten mit V24-Anschluß und dem LSI11-Bus (Q-Bus).

Werden 20 mA Stromschleifen benötigt, so ist ein zusätzlicher Konverter (DLV11-KA) zu installieren.

### Features

- Vier unabhängige serielle Kanäle in einem Bus-Device
- Kompatibilität mit serieller EIA RS-232C und RS-423, AS-422 oder 20 mA Stromschleife (abhängig von Kanalkonfiguration und Kabelauswahl)
- Alle Kanäle können unabhängig voneinander konfiguriert werden:
  - für quarzgesteuerte Baud-Raten:  
150, 300, 600, 1200, 2400, 4800, 9600,  
19200 oder 38400 Bits pro Sekunde. Bei Anwendung der DLV11-KA Option sind 110 Bit/s verfügbar
  - für Zeichenformate:  
7 oder 8 Datenbits, 1 oder 2 Stopbits, bei Bedarf Parität (ungerade oder gerade)
- Kanal 3 kann dem Bildschirminterface gewidmet werden.
- Kanal 3 kann bei Empfang eines 'breaks' entweder in den Halt-Mode gehen oder einen Bootstrap durchführen (auch keine Antwort ist möglich).
- Hard- und Softwareäquivalenz mit vier DLV11en

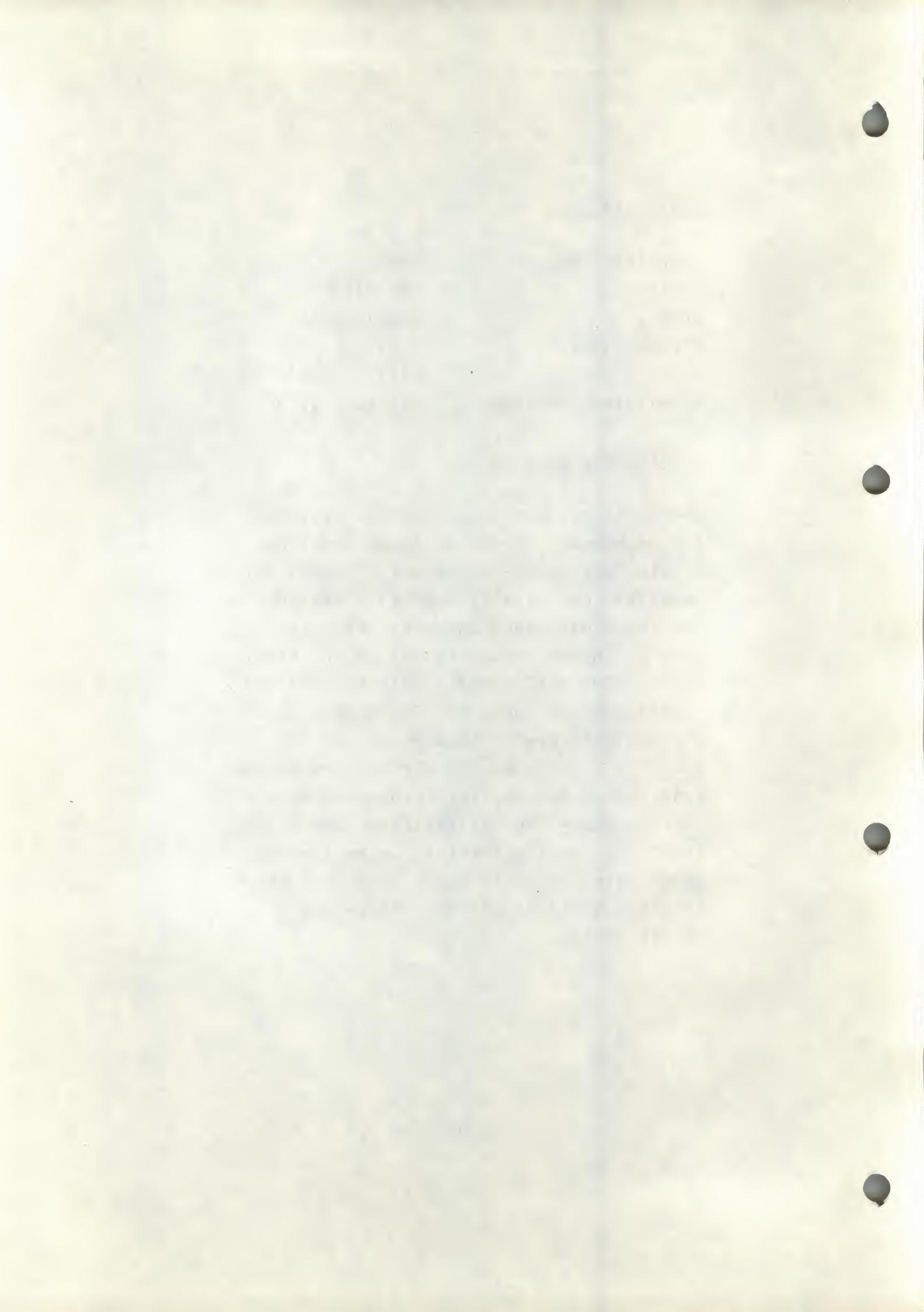


## Spezifikationen

Identifikation	M8043
PCS-Nummer	900.610
Größe	Double Slot
Stromversorgung	+ 5V / 1 A +12V / 0,25A
normierte Busbelastung	1,0 AC, 1,0 DC

## Funktionsbeschreibung

Die DLV11-J dient als Interface zwischen 4 asynchronen, seriellen Kommunikationskanälen und dem Q-Bus. Sie führt Seriell/Parallel- und Parallel/Seriell-Datenkonversionen mit einem universellen asynchronen Empfänger/Sender (UART) pro Kanal durch. Der UART enthält alle Sender- und Empfängerfunktionen. Der Empfänger führt die Seriell/Parallel-Konversion von 7- oder 8-Bit-Codes durch, die Zeichen erscheinen im Datenpuffer rechtsbündig ohne Start-, Stop- und Paritätsbits. Der Sender führt die Parallel/Seriell-Konversion der Daten, die vom LSI11-Bus kommen, aus und versieht diese mit Start-, Stop- und Paritätsbits.



## Register

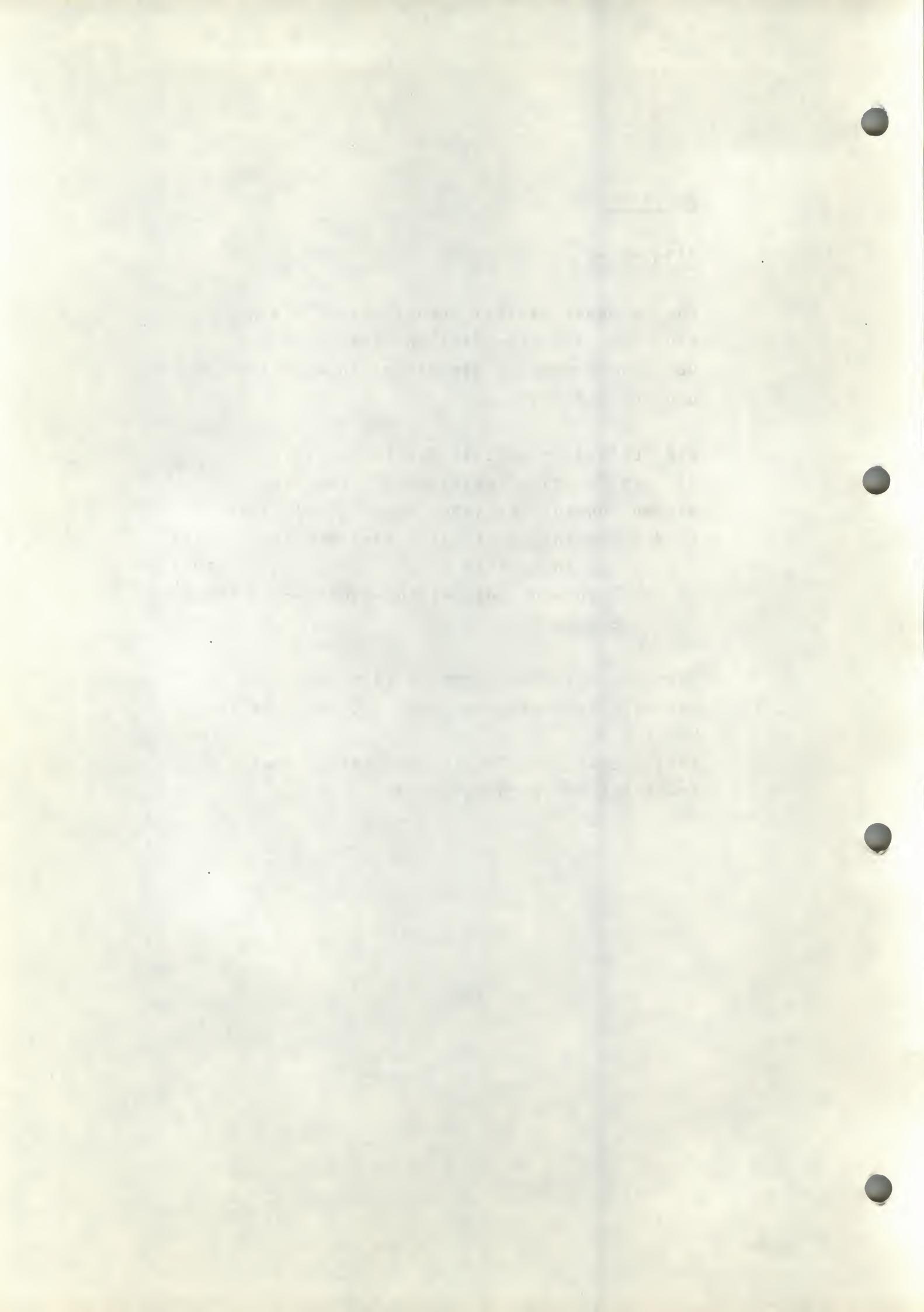
### Allgemeines

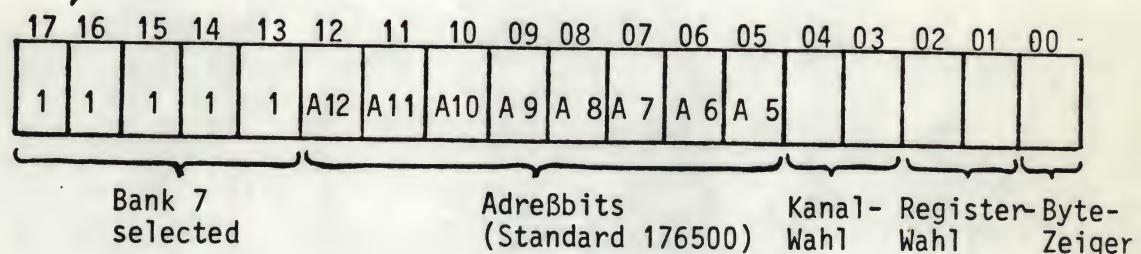
Das folgende Kapitel enthält die für den Programmierer erforderliche Information über die Bedeutung der einzelnen Register und ihrer Bits.

Die DLV11-J enthält 16 Device-Register, die vom Programm individuell adressiert werden können. Für jeden Kanal (0-3) gibt es die Empfangs-Kontroll/Status-Register (RCSR)  
Empfangsbuffer (RBUF)  
Sende-Kontroll/Status-Register (XCSR)  
Sendebuffer (XBUF)

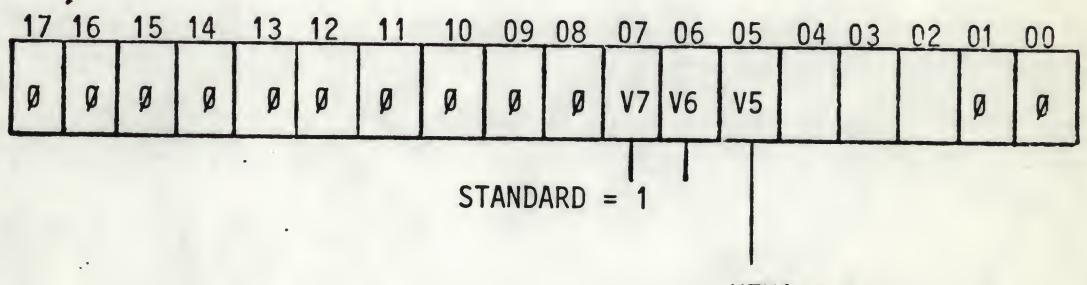
Über die Wire-Wrap-Jumpers lässt sich eine Basisadresse erzeugen. Dies ist das RCSR im Kanal Ø.

Bild 1 zeigt das Format der Device-Adresse sowie das Vektorformat.



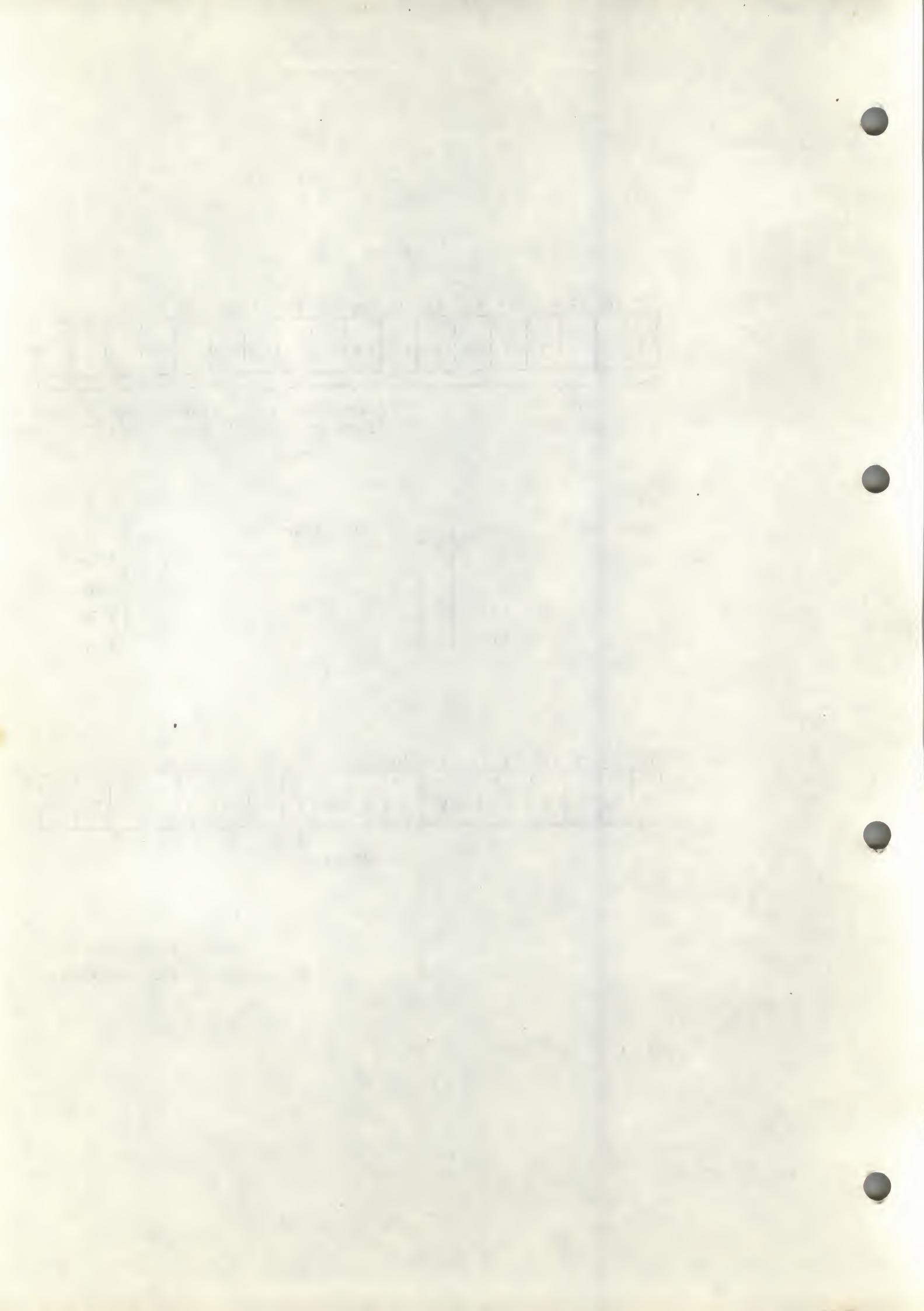


Kanal-Wahl:	Adresse	Kanal	Register-Wahl:	Adresse	Register
	00	0		00	RCSR
	01	1		01	RBUF
	10	2		10	XCSR
	11	3		11	XBUF



XZU1 = 1  
 XZU0 = Ø mit Konsole  
 keine Verb. = Ø ohne Konsole

Bild 1

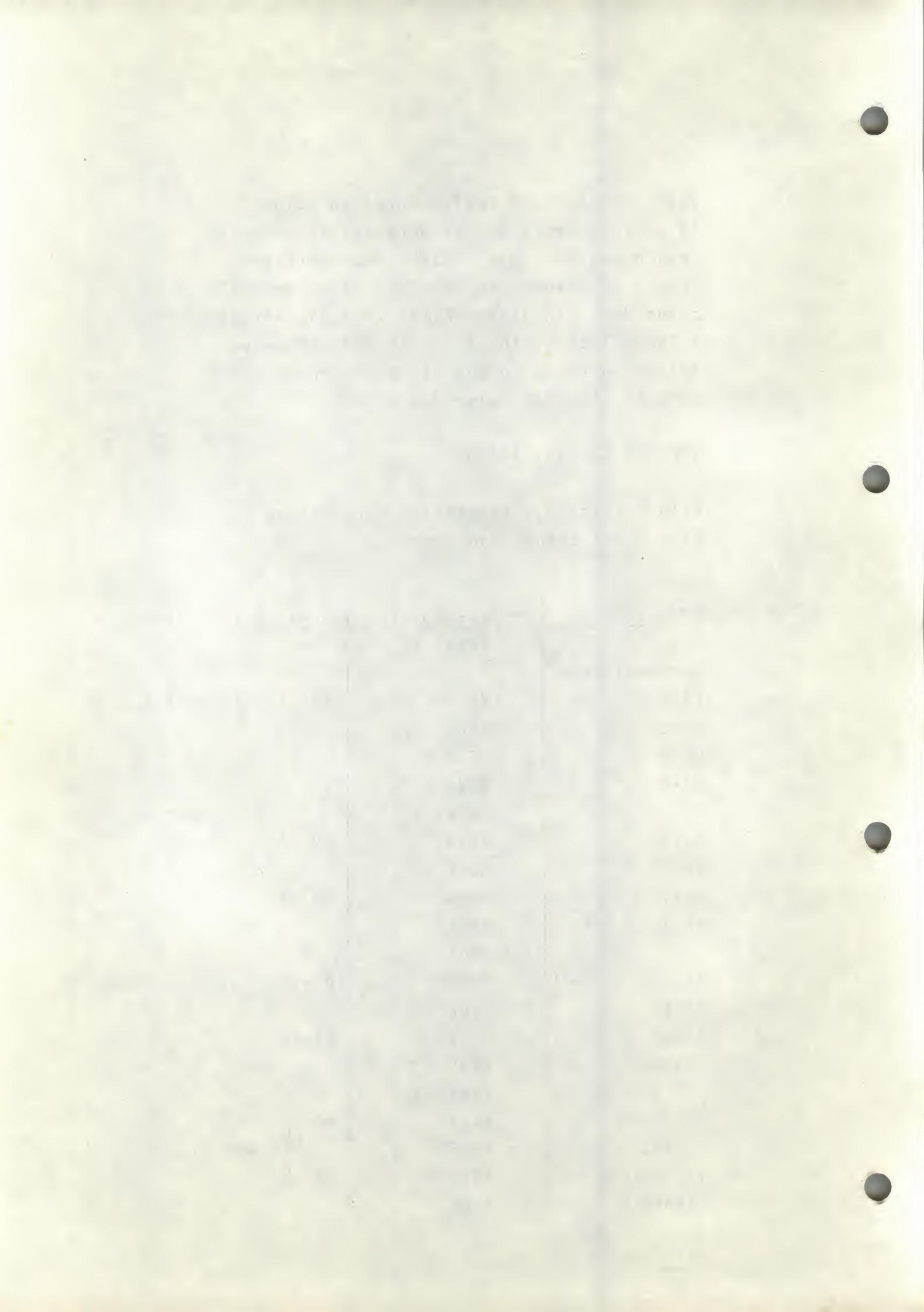


Die verbleibenden Device-Adressen folgen in 16 aufeinanderfolgenden Wortadressen. Es ist jedoch möglich, die letzten vier Adressen (Kanal 3) unabhängig dem Bildschirmterminal zuzuordnen. In diesem Falle wird die Adresse 177560-177566 sein. Soll ein Bildschirm betrieben werden, so muß die Device-Basis-Adresse eine der folgenden sein:

176500, 176540, 177500

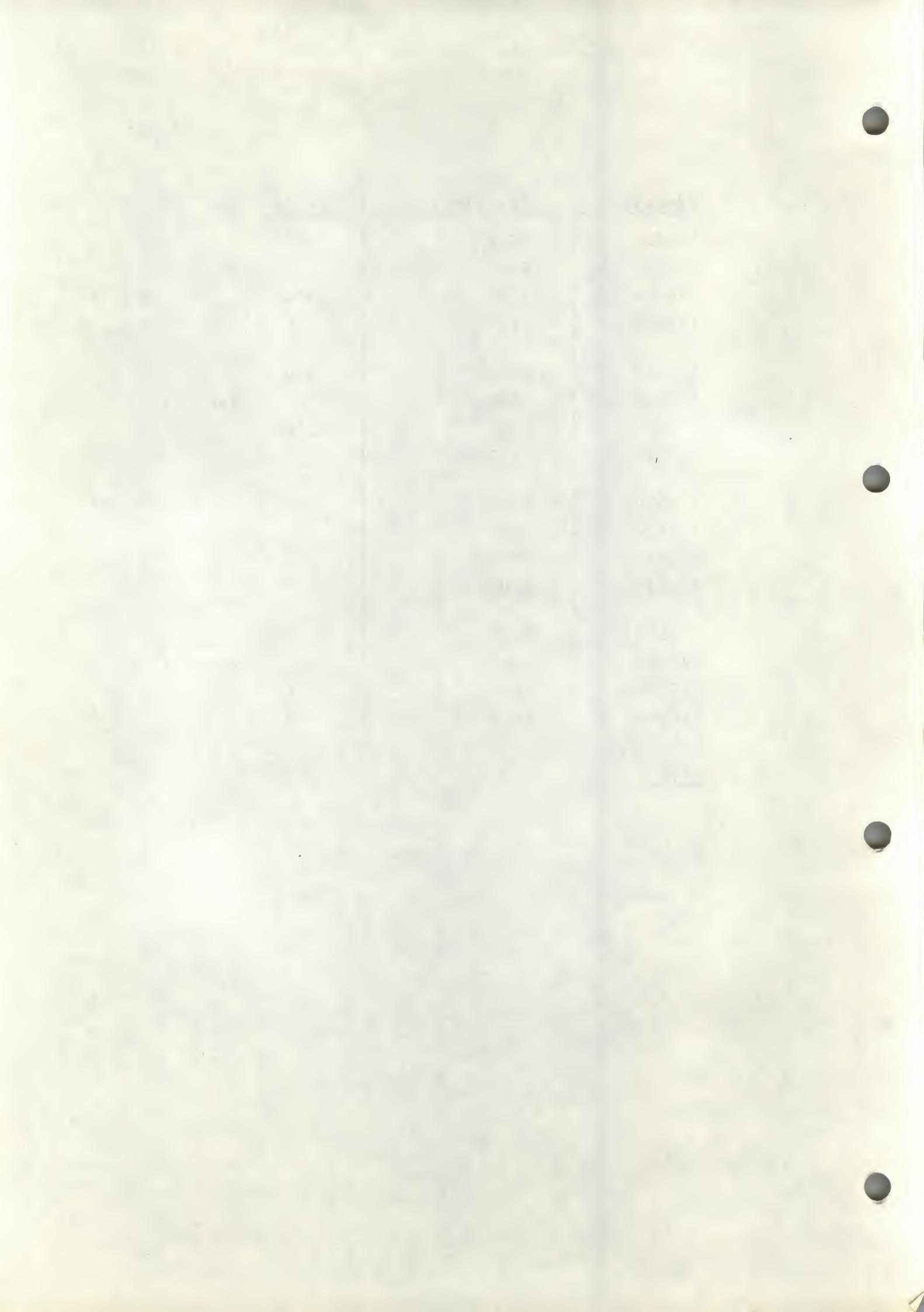
Bild 2 zeigt die allgemeine Adreßbelegung, Bild 3 die Standardadressen.

Adresse	Device-Register	zugeordneter Vektor
	Kanal 0	
<b>Basis-Adresse</b>		
(BA)	RCSR	Basis-Vektor (BV)
BA+2	RBUF	
BA+4	XCSR	BV+4
BA+6	XBUF	
	Kanal 1	
BA+10	RCSR	BV+10
BA+12	RBUF	
BA+14	XCSR	BV+14
BA+16	XBUF	
	Kanal 2	
BA+20	RCSR	BV+20
BA+22	RBUF	
BA+24	XCSR	BV+22
BA+26	XBUF	
	Kanal 3	
177560	RCSR	60 ]
177562	RBUF	
177564	XCSR	64 ] Konsole
177566	XBUF	



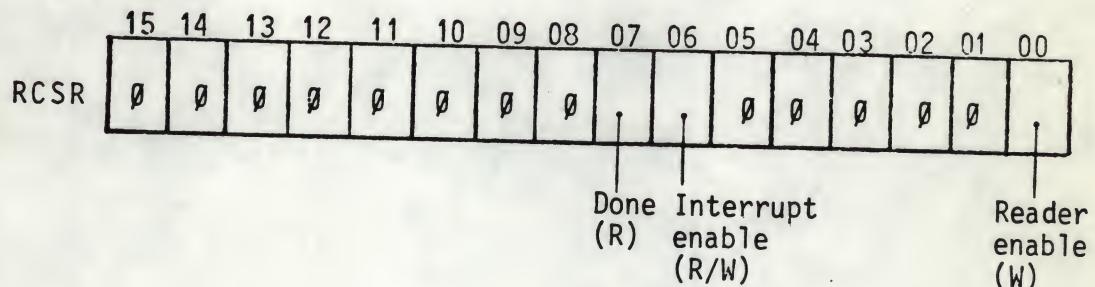
Adresse	Register	Vektor
176500	RCSR	300
176502	RBUF	Kanal 0
176504	XCSR	304
176506	XBUF	
176510	RCSR	310
176512	RBUF	Kanal 1
176514	XCSR	314
176516	XBUF	
176520	RCSR	320
176522	RBUF	Kanal 2
176524	XCSR	324
176526	XBUF	
176560	RCSR	60
176562	RBUF	Kanal 3
176564	XCSR	64
176566	XBUF	

Bild 3

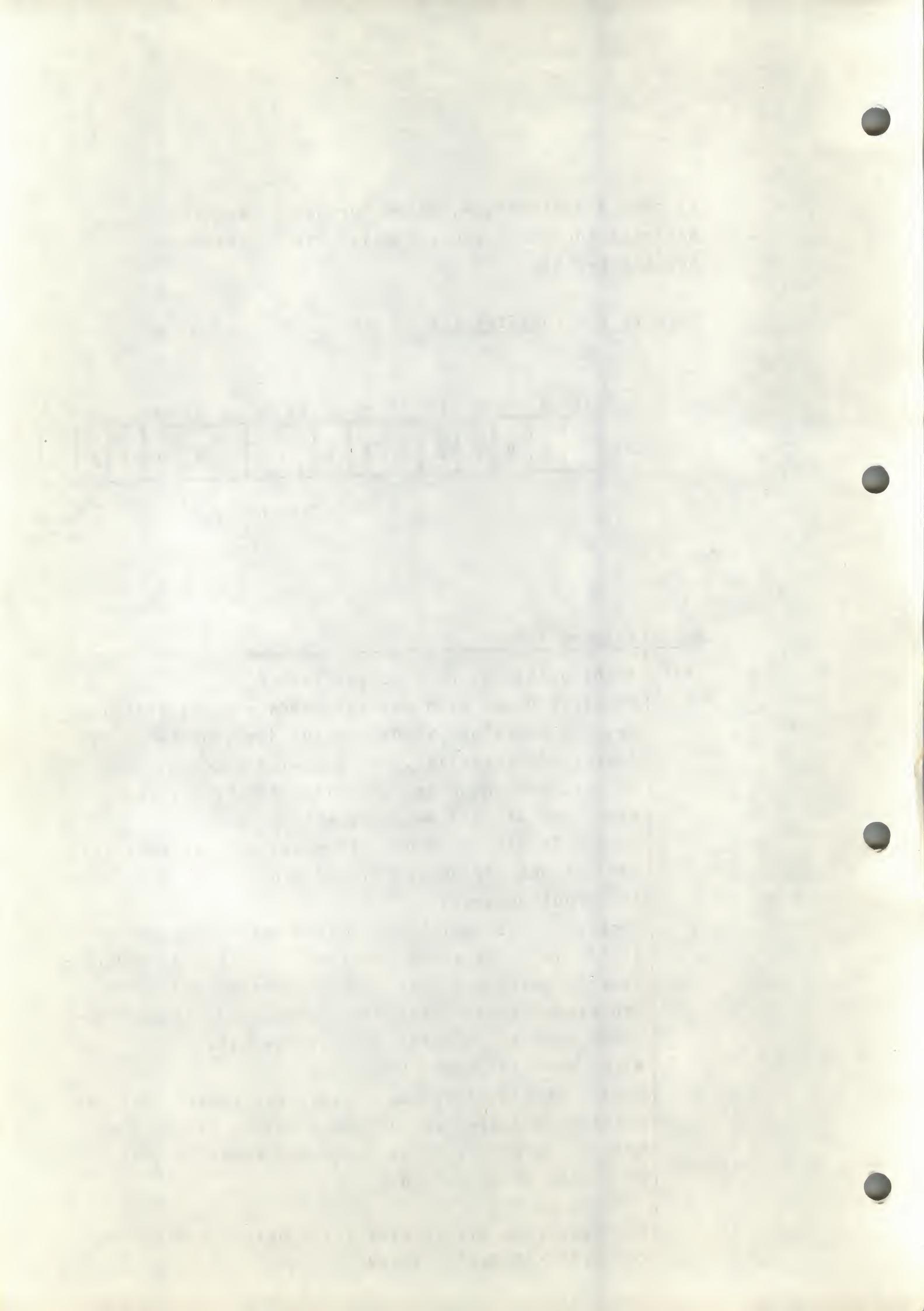


Es gibt 4 Wortformate, eines für jedes Device-Register innerhalb eines Kanals, die im folgenden beschrieben sind.

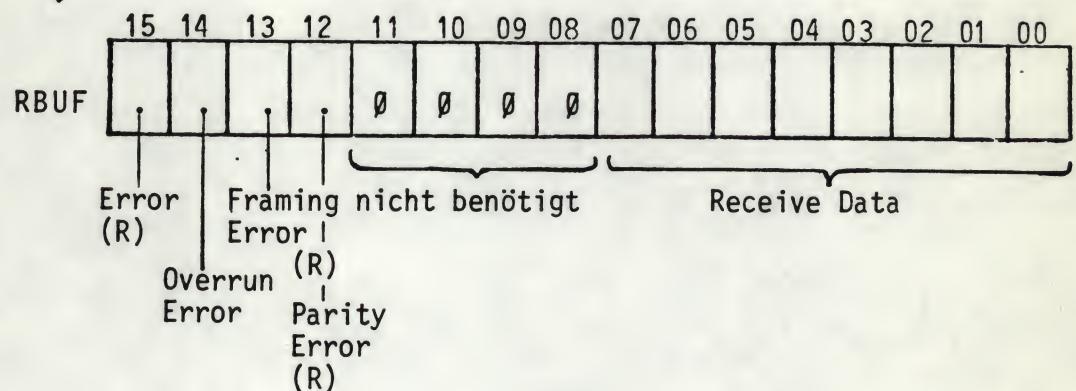
#### Receive Control/Status-Register



Bit	Beschreibung
8/15	Nicht benötigt. Beim Schreiben = Ø
7	Receiver Done. Wird gesetzt, wenn ein vollständiges Zeichen empfangen wurde und für die Eingabe in den Prozessor bereit ist. Das Bit wird automatisch gelöscht, wenn RBUF gelesen wird, BINITL angelegt wird oder das Bit Reader Enable gesetzt ist. Read Only Bit. Wenn das Bit 6 des RCSR gesetzt ist, bewirkt das Setzen des Bits 7 den Einsprung in eine Interrupt-Sequenz.
6	Receiver Interrupt Enable. Wird unter Programmkontrolle im Falle einer Receiver Interrupt Anforderung gesetzt (wenn ein Zeichen zur Übertragung in den Prozessor bereit ist). Wird gelöscht durch das Programm oder durch BINIT. Read/Write Bit.
1-5	Nicht benötigt. Beim Lesen = Ø
Ø	Reader Enable. Indem man dieses Bit setzt, geht der Lochstreifenleser am LT33-Terminal um ein Zeichen weiter. Durch das Setzen wird das Done-Bit (Bit 7) gelöscht. Write Only Bit.  Die Benutzung dieses Bits setzt das Vorhandensein der DLV11-KA-Option voraus.



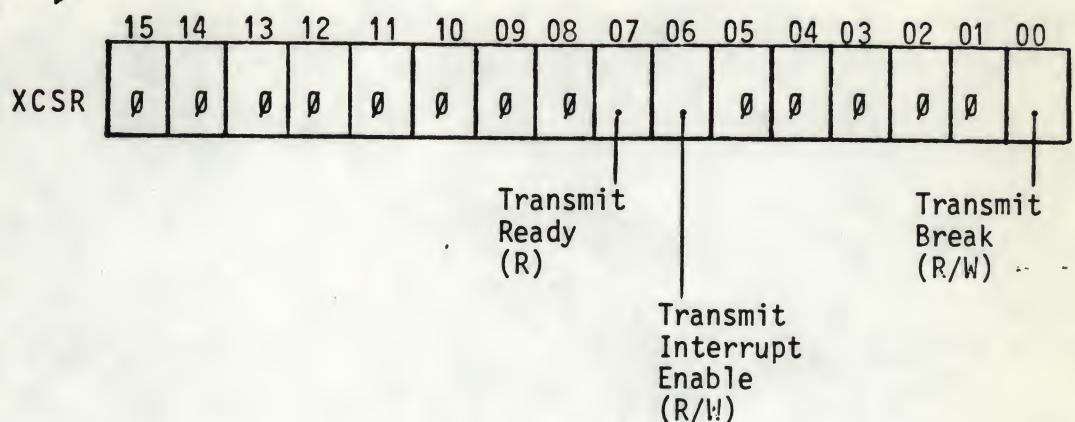
### Receive Buffer



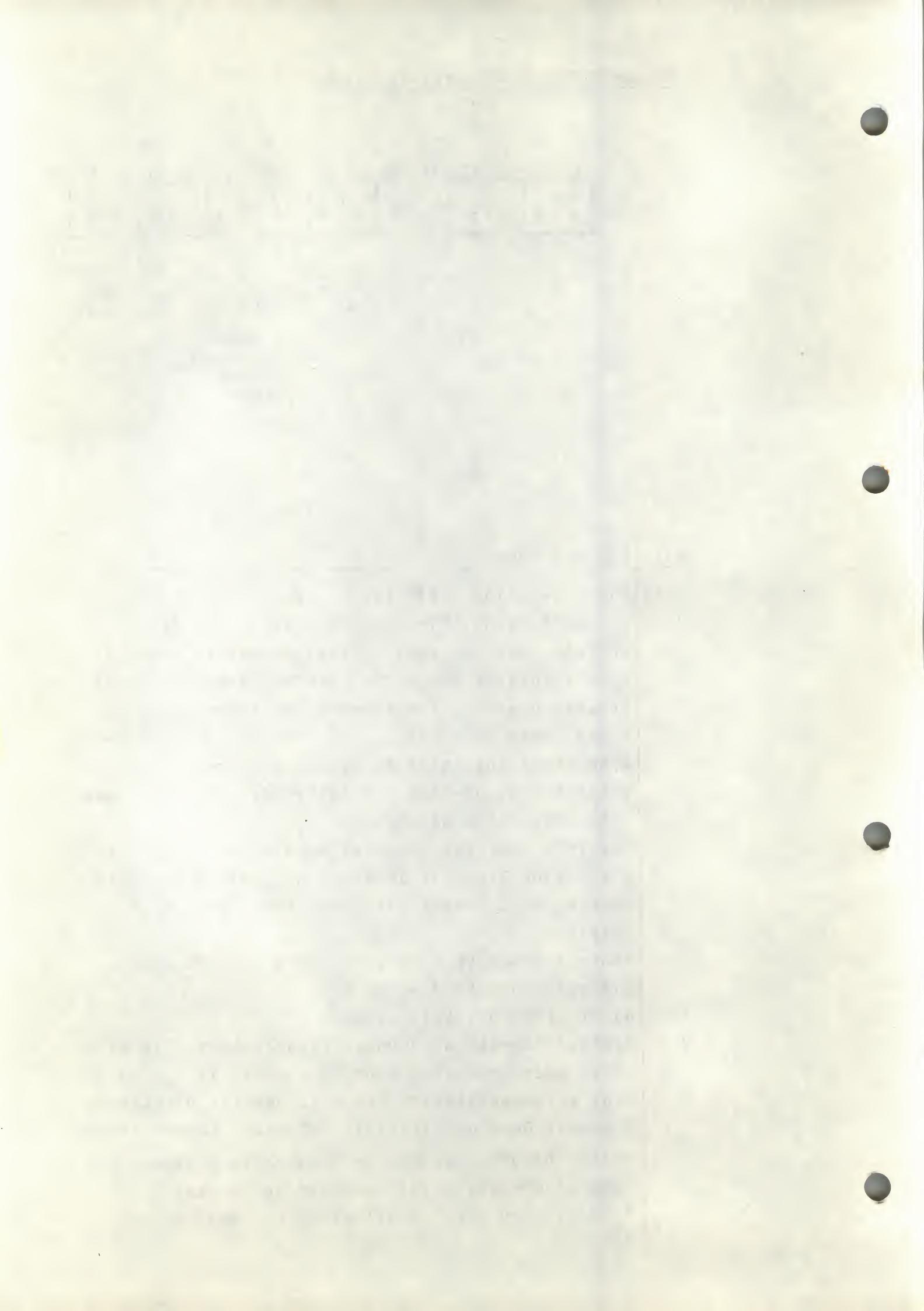
Bit	Beschreibung
15	Channel Error Status. Logisches 'OR' aus Bit 14,13 und 12. Read Only Bit.
14	Overrun Error. Wenn dieses Bit gesetzt ist, wird angezeigt, daß das Lesen eines Datums vor dem Senden eines neuen nicht beendet wurde. Wird durch BINIT gelöscht. Read Only Bit.
13	Framing Error. Das gesetzte Bit zeigt beim gelesenen Zeichen ein ungültiges Stop-Bit an. Wird durch BINIT gelöscht. Read Only Bit.
12	Parity Error. Die empfangene Parität stimmt nicht mit der erwarteten überein, wenn dieses Bit gesetzt ist. Falls das Device ohne Parität betrieben wird, ist dieses Read Only Bit immer Ø.
8-11	Nicht benötigt. Beim Lesen = Ø
Ø-7	Daten-Bits. Enthält 7 oder 8 Bits rechtsbündig. Read Only Bits.

1. The first step in the process of determining the  
2. relationship between the two variables is to  
3. collect data on both variables. This can be done  
4. through observation, experiments, or surveys.  
5. Once data has been collected, it is important to  
6. organize and analyze the data. This involves  
7. calculating descriptive statistics such as mean,  
8. median, mode, and standard deviation. It also  
9. involves creating graphs and charts to visualize  
10. the data and identify patterns or trends.  
11. After the data has been analyzed, the next step  
12. is to determine the type of relationship between  
13. the two variables. This can be done by  
14. calculating correlation coefficients or regression  
15. equations. Correlation coefficients measure  
16. the strength and direction of the relationship  
17. between two variables, while regression  
18. equations can be used to predict the value of one  
19. variable based on the value of another.  
20. Finally, it is important to interpret the results  
21. of the analysis and draw conclusions about  
22. the relationship between the two variables.  
23. In conclusion, determining the relationship  
24. between two variables requires collecting  
25. data, organizing and analyzing the data,  
26. determining the type of relationship, and  
27. interpreting the results.

## Transmit Control/Status-Register

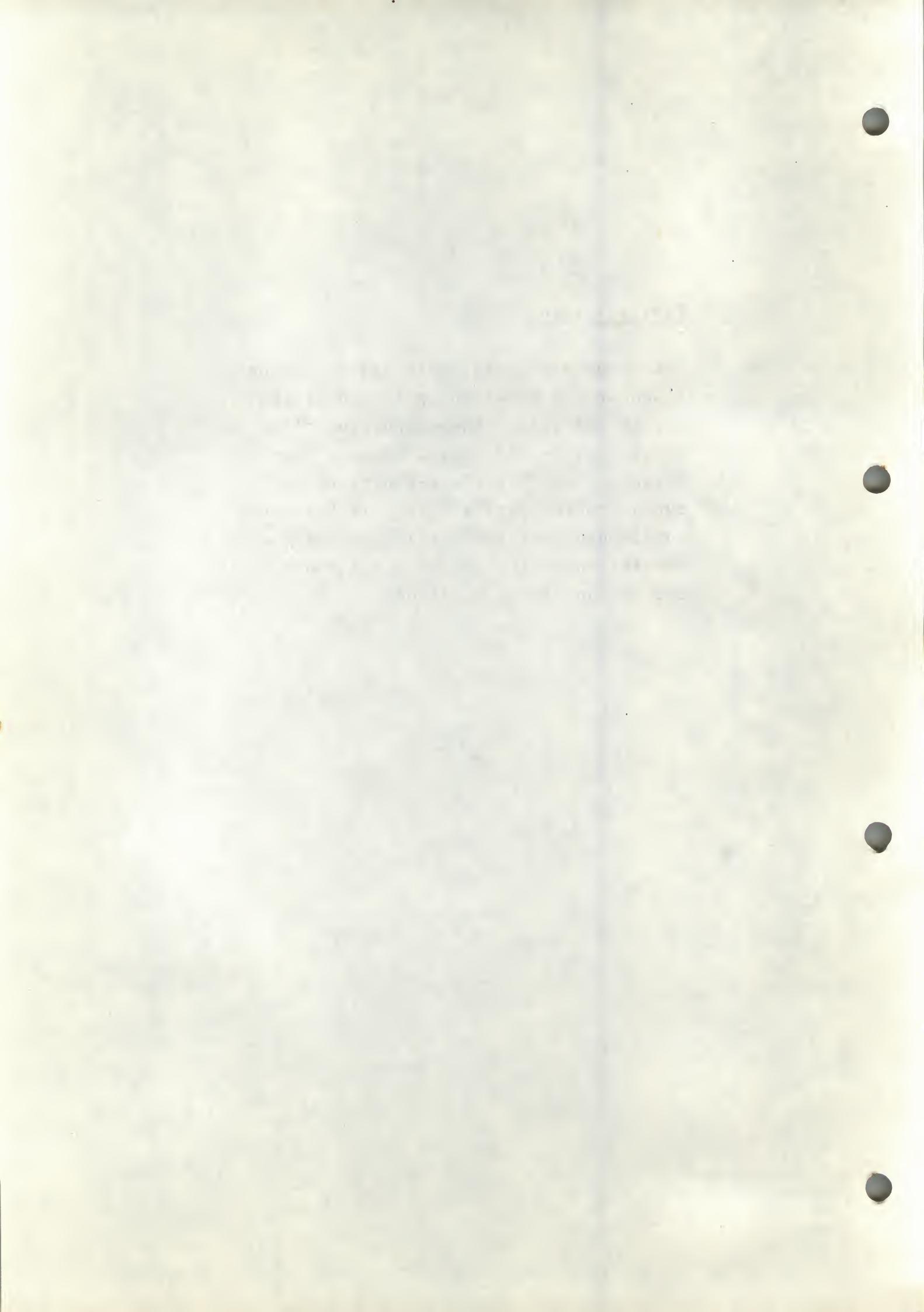


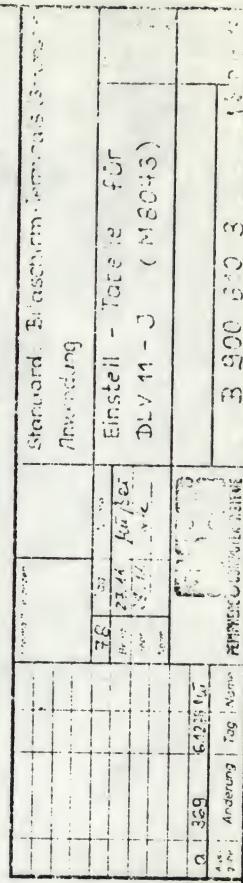
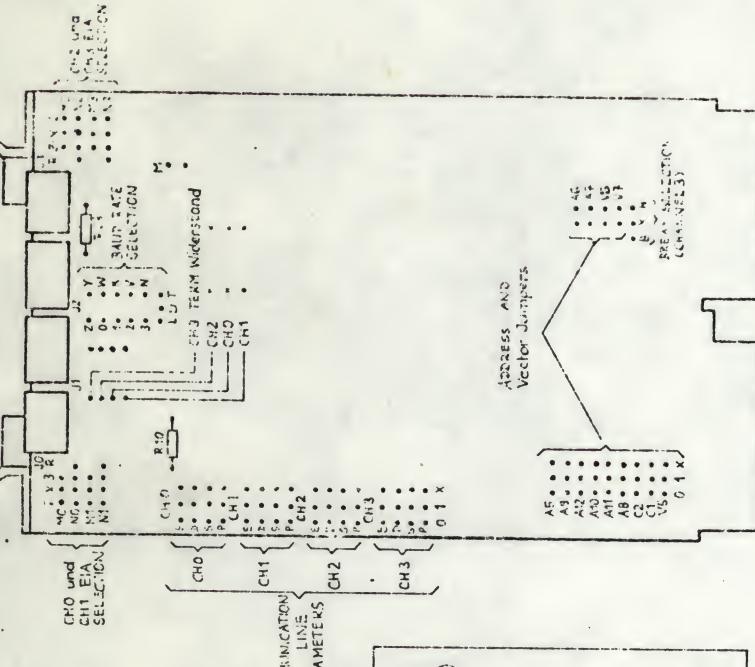
Bit	Beschreibung
8-15	Nicht benötigt. Beim Lesen = Ø
7	Transmit Ready. Wird gesetzt, wenn XBUF leer ist und ein neues Zeichen übertragen werden kann. Es wird ebenfalls durch INIT während einer Power-Up-Sequenz oder während einer Reset-Instruction gesetzt. Read Only Bit. Wenn das Transmitter Interrupt Enable Bit (Bit 6) gesetzt ist, bewirkt das Setzen des Transmit Ready Bits eine Interrupt-Sequenz.
6	Transmit Interrupt Enable. Wenn es erforderlich wird, eine Transmit Interupt Anforderung zu generieren, wird dieses Bit unter Programmkontrolle gesetzt. Während Power-Up oder Init-Function wird dieses Bit gelöscht. Read/Write Bit.
1-5	Nicht benötigt. Beim Lesen = Ø
Ø	Transmit Break. Wird unter Programmkontrolle gesetzt oder gelöscht. Wenn es gesetzt ist, wird eine zusammenhängende Leerzeichenkette übertragen. Transmit Done und Transmit Interrupt können jedoch weiter benutzt werden. Im gelöschten Zustand kann eine normale Zeichenübertragung stattfinden. Wird durch BINIT gelöscht. Read/Write Bit.



## Einstellungen

Das folgende Kapitel beschreibt, wie der Anwender das Modul entsprechend seinem System und seiner Anwendung einstellen kann. Register-Adressen, Vektor-, Übertragungs- und Interface-Funktionen sind durch Brücken einstellbar. Die Standard-adreß- und Vektoreinstellung enthält nachfolgende Tabelle, ebenso die der Brücken und deren Position.





R = entfernt  
J = eingesetzt



## UART-Funktionen

Die Funktion des UARTs (universeller asynchroner Empfänger und Sender) werden durch die Brücken D, S, P und E eingestellt - gemäß folgender Tabelle.

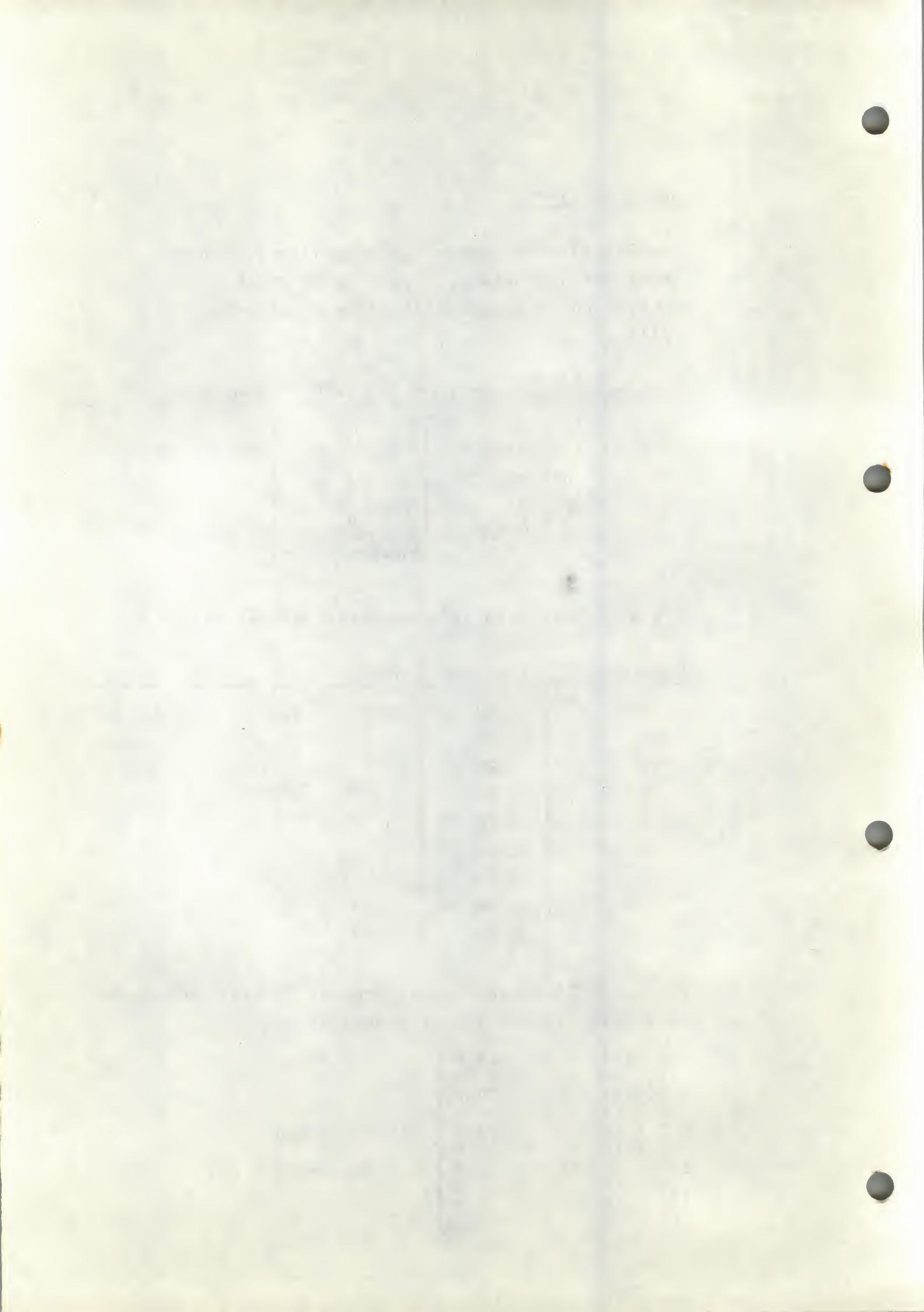
Bezeichnung	Kanal Parameter	X ZU Ø	X ZU 1	Bemerkungen
D	Nr. Datenbits	7	8	LSB zuerst übertragen
S	Nr. Stopbits	1	2	
P	Parität	Parität	keine	
E	gerade Parität	Ungerade erwartet	Gerade erwartet	Nur wenn P = Ø

Die Baud-Rate wird folgendermaßen eingestellt.

Bezeichnung	Baud-Rate	Brücke
U	150	nach Ø, 1, 2, 3 (Ø, 1, 2, 3 = Kanäle)
T	300	"
V	600	"
W	1 200	"
Y	2 400	"
L	4 800	"
N	9 600	"
K	19 200	"
Z	38 400	"

Zur Einstellung der Signalform bei den verschiedenen Baud-Raten sind folgende Widerstände nötig:

38,4 KB	22 K	R10 für CHØ und CH1
19,2 KB	51 K	
9,6 KB	120 K	
4,8 KB	200 K	
2,4 KB	430 K	
1,2 KB	820 K	
600 KB	1 M	R23 für CH2 und CH3
300 KB	1 M	
150 KB	1 M	
110 KB	1 M	



Bei Benutzung des Kanals 3 als Konsolenkanal lässt sich ein 'Break' folgendermaßen verarbeiten:

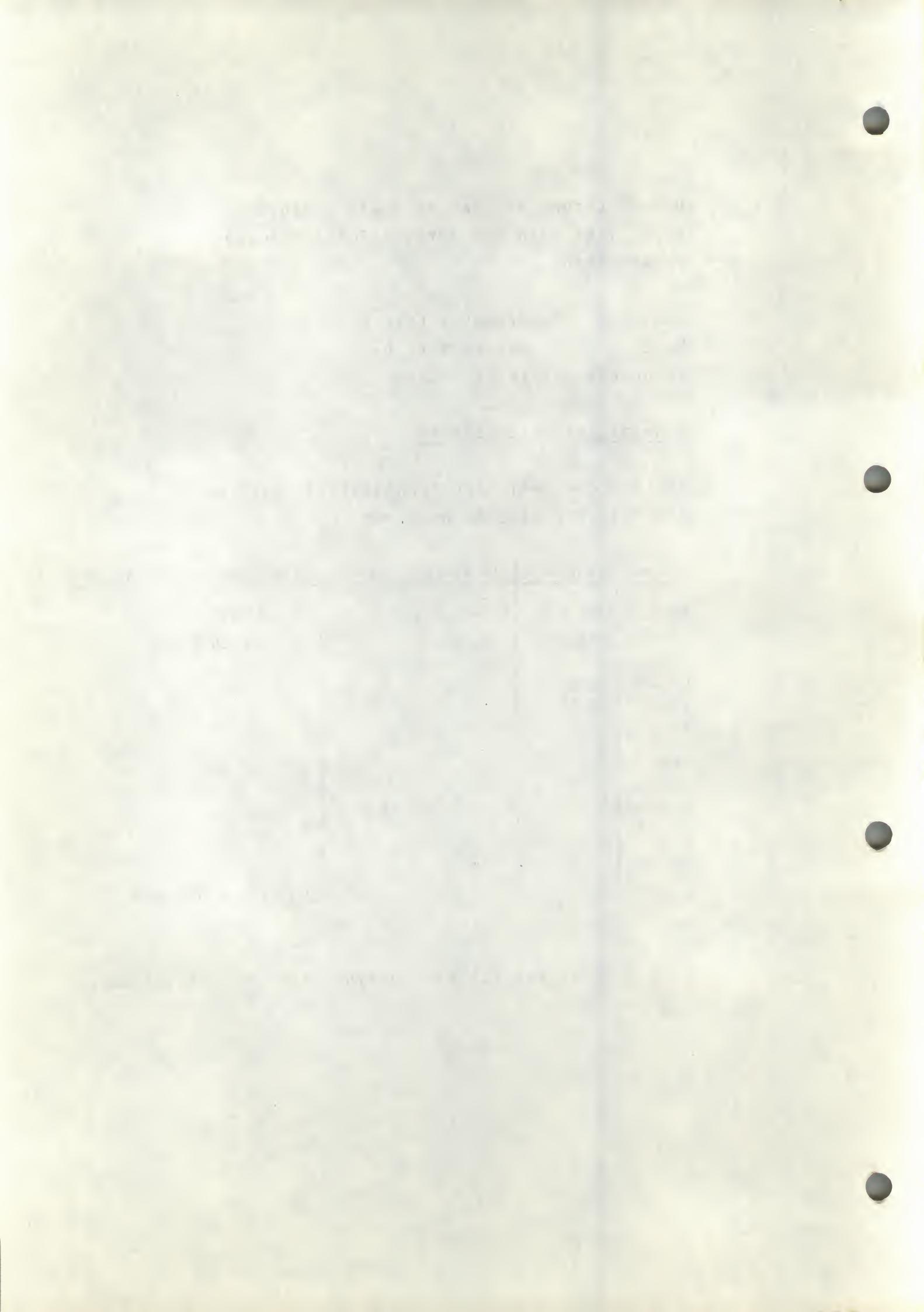
Boot	Brücke X nach B
Halt	Brücke X nach H
keine Antwort	keine Brücke

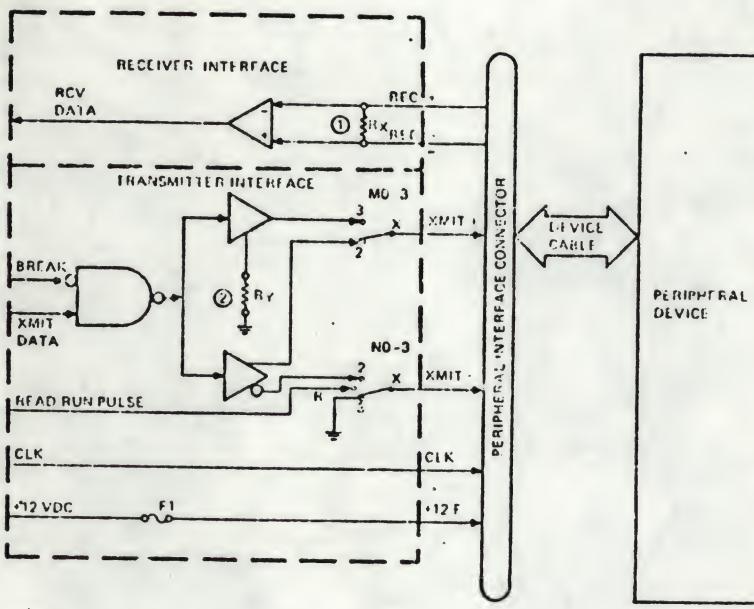
#### Schnittstellenfunktionen

Die Art der seriellen Schnittstelle wird durch die folgende Tabelle bestimmt:

Brücke	EIA RS-422	EIA RS-232C, RS-423	20mA Stromschleife mit DLV11-KA
MØ-3	X nach 2	X nach 3	X nach 3
NØ-3	X nach 2	X nach 3	X nach R
Anschluß Wider- stand (einer pro Kanal)	100 1/4W		
Signal- formung (einer pro Paar)		nach obiger Tabelle	
Fuse 1			1,0 A Pico Fuse

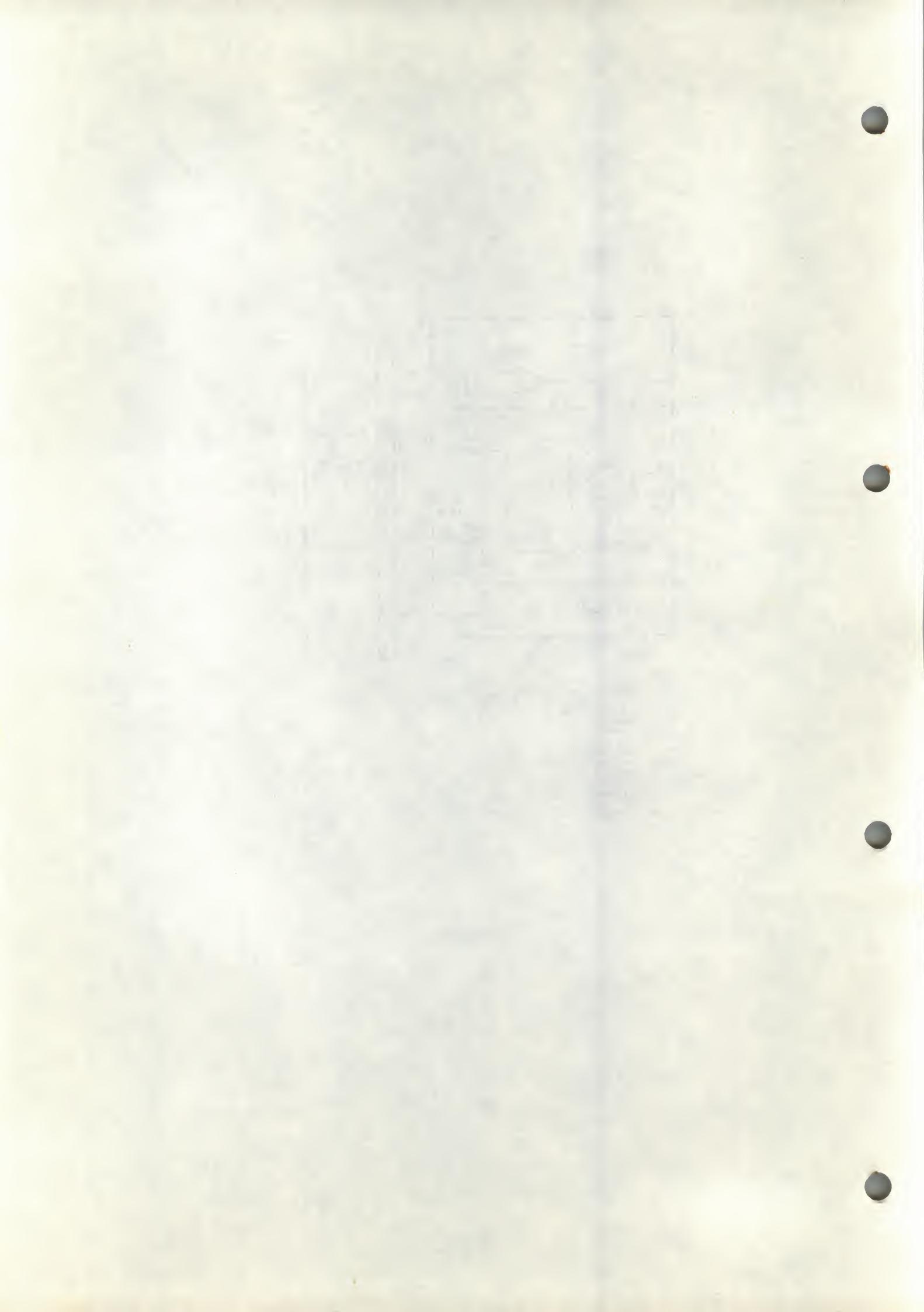
Bild 4 zeigt das Schaltbild eines typischen Interfaces.

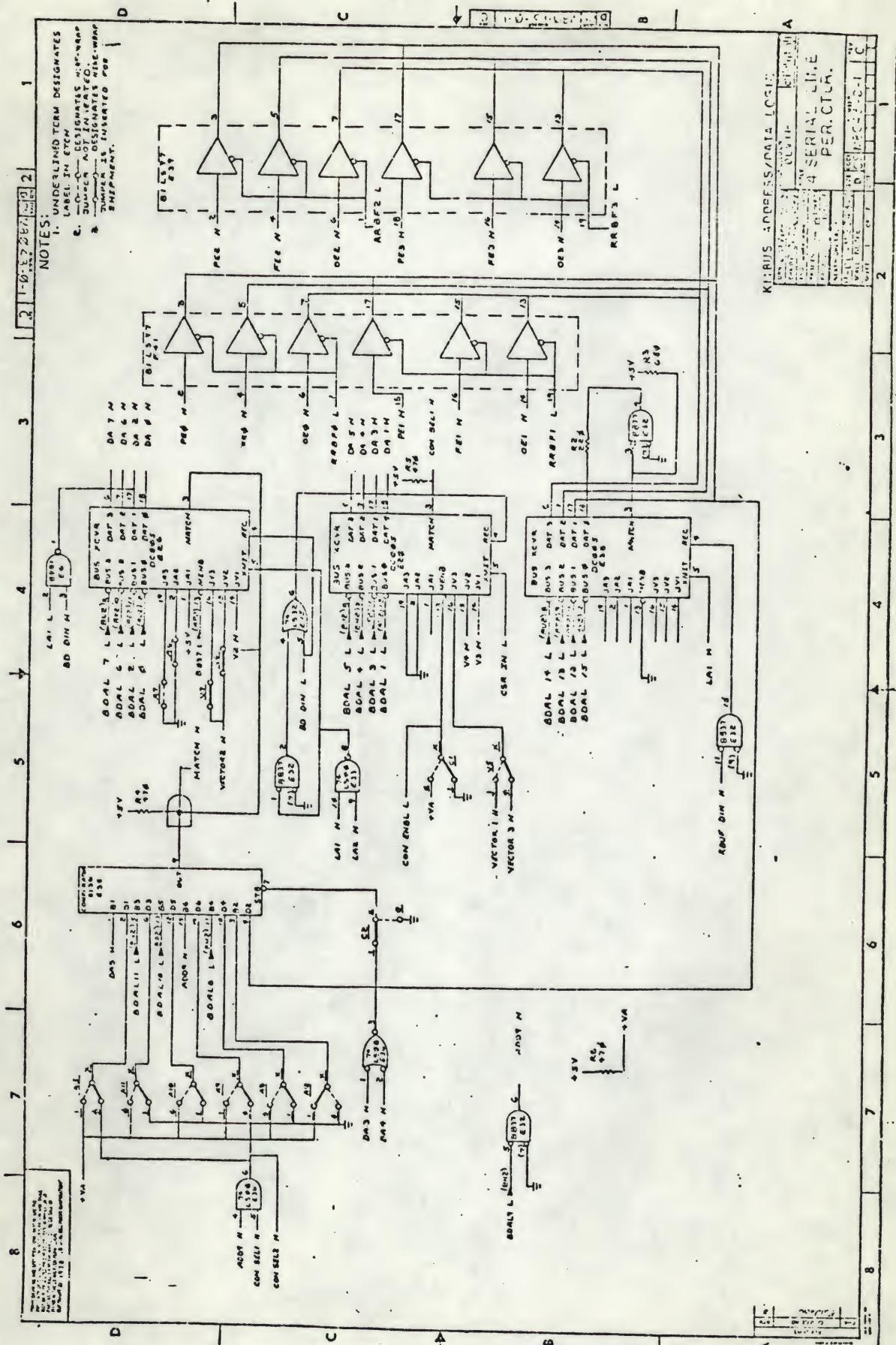


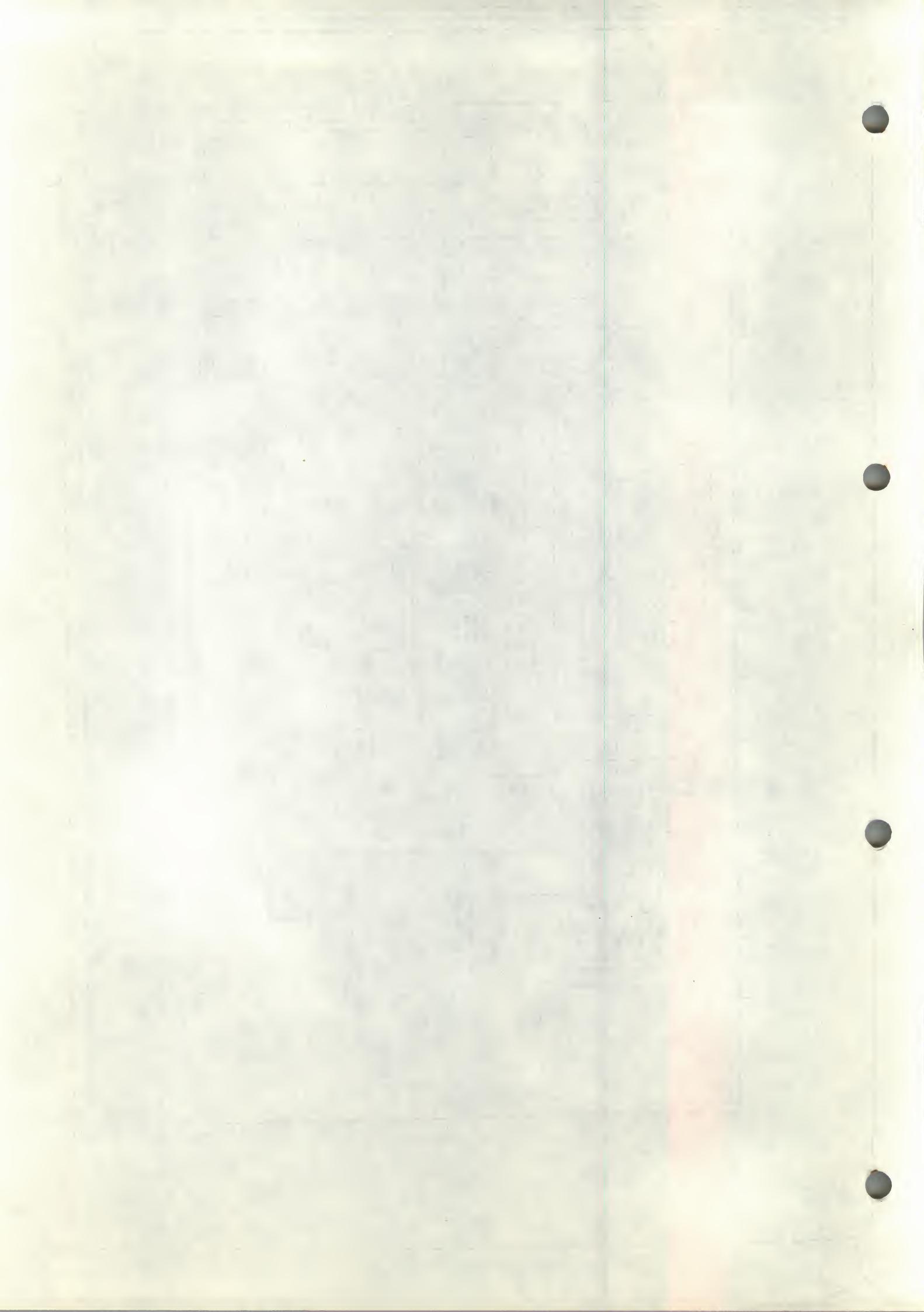


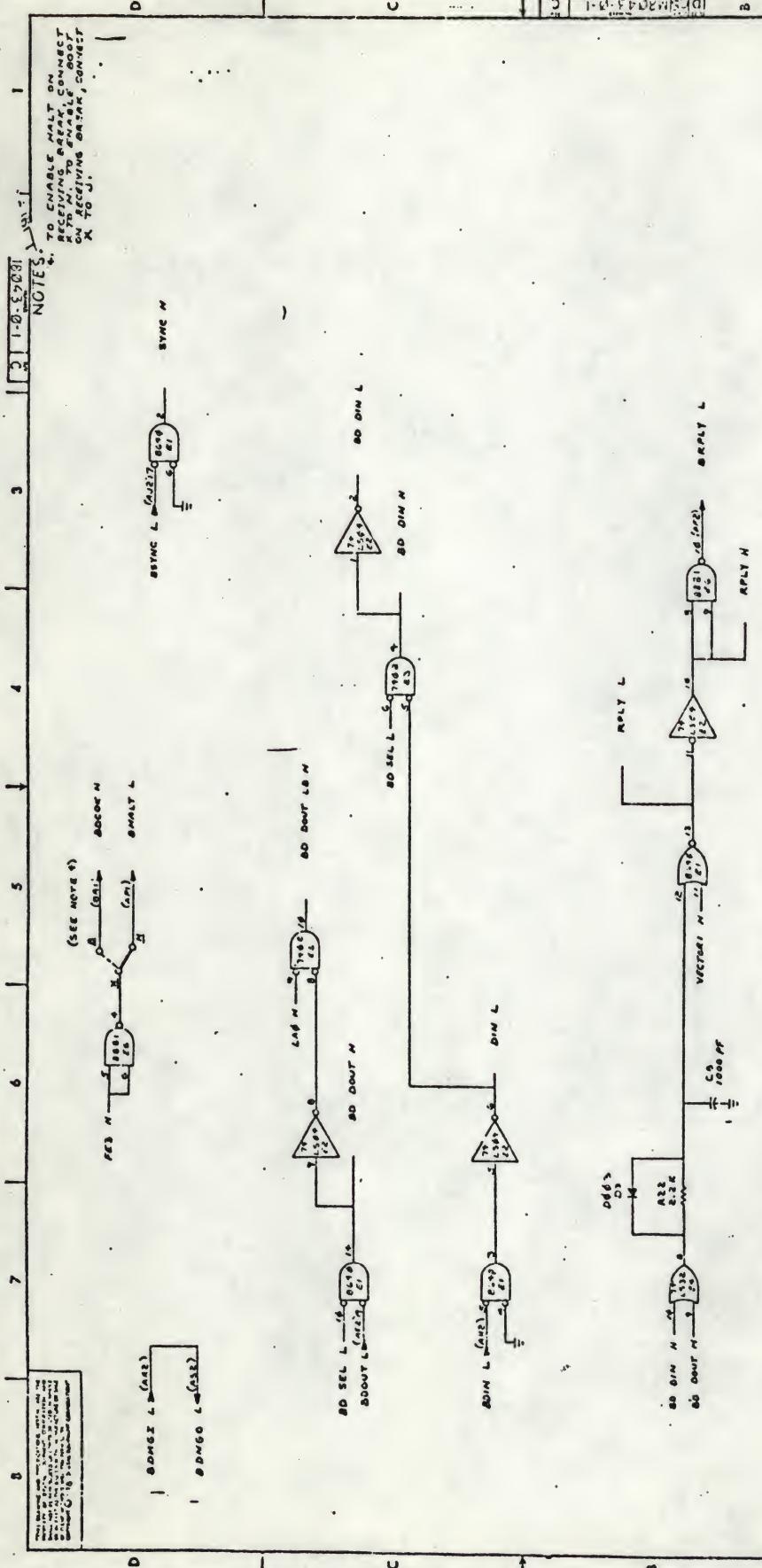
NOTES

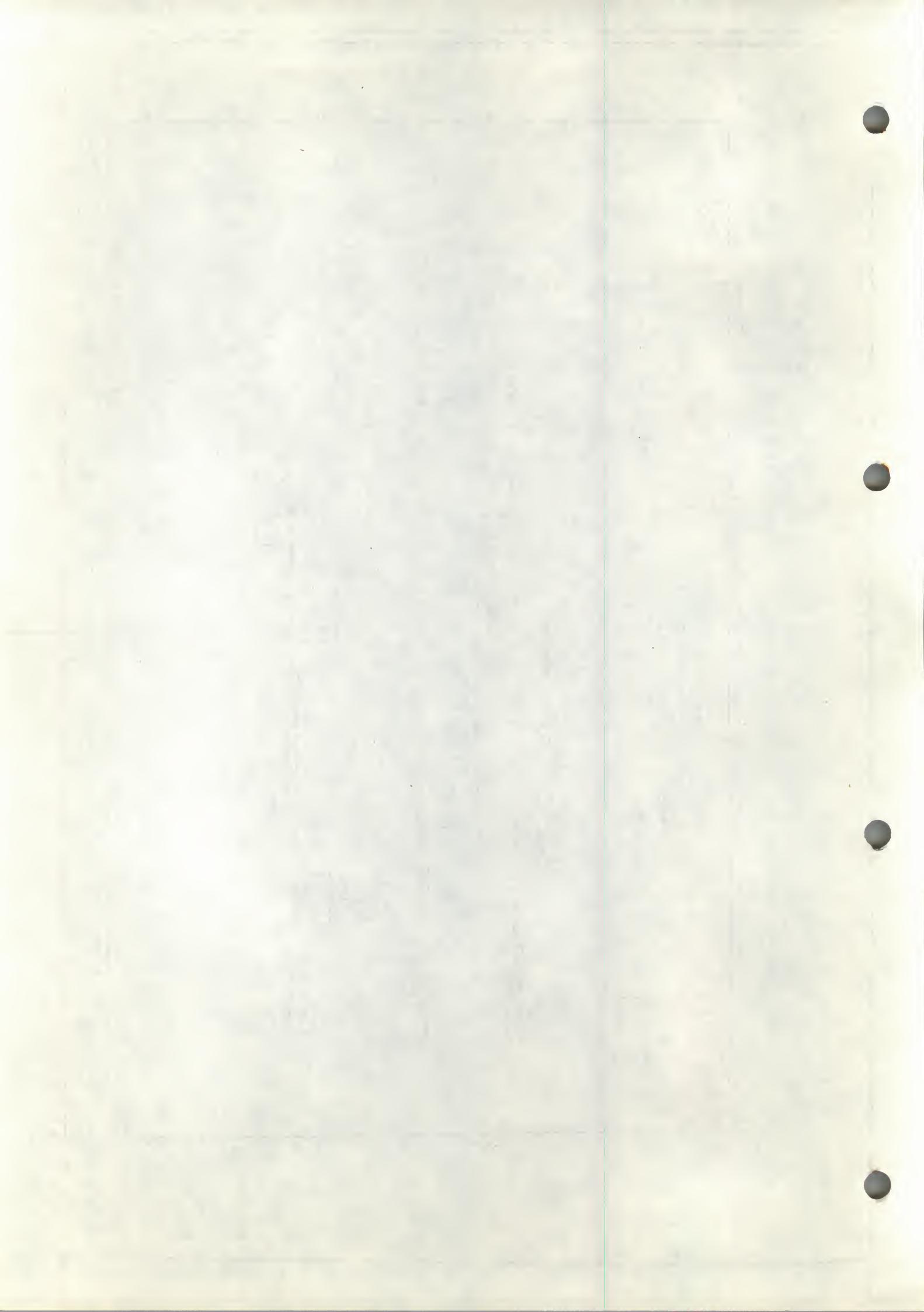
- ① RX IS INSTALLED WHEN CHANNEL IS CONFIGURED FOR EIA RS 422 OPERATION (100 Ω, 1.4 W NON WIRE WOUND)  
R30 - CHANNEL 0  
R31 - CHANNEL 1  
R32 - CHANNEL 2  
R33 - CHANNEL 3
- ② RX IS CHOSEN FOR PROPER SLEW RATE WHEN CHANNEL IS CONFIGURED FOR EIA RS 232C/RS 423 OPERATION  
R10 SETS SLEW RATE FOR CHANNELS 0 AND 1  
R23 SETS SLEW RATE FOR CHANNELS 2 AND 3

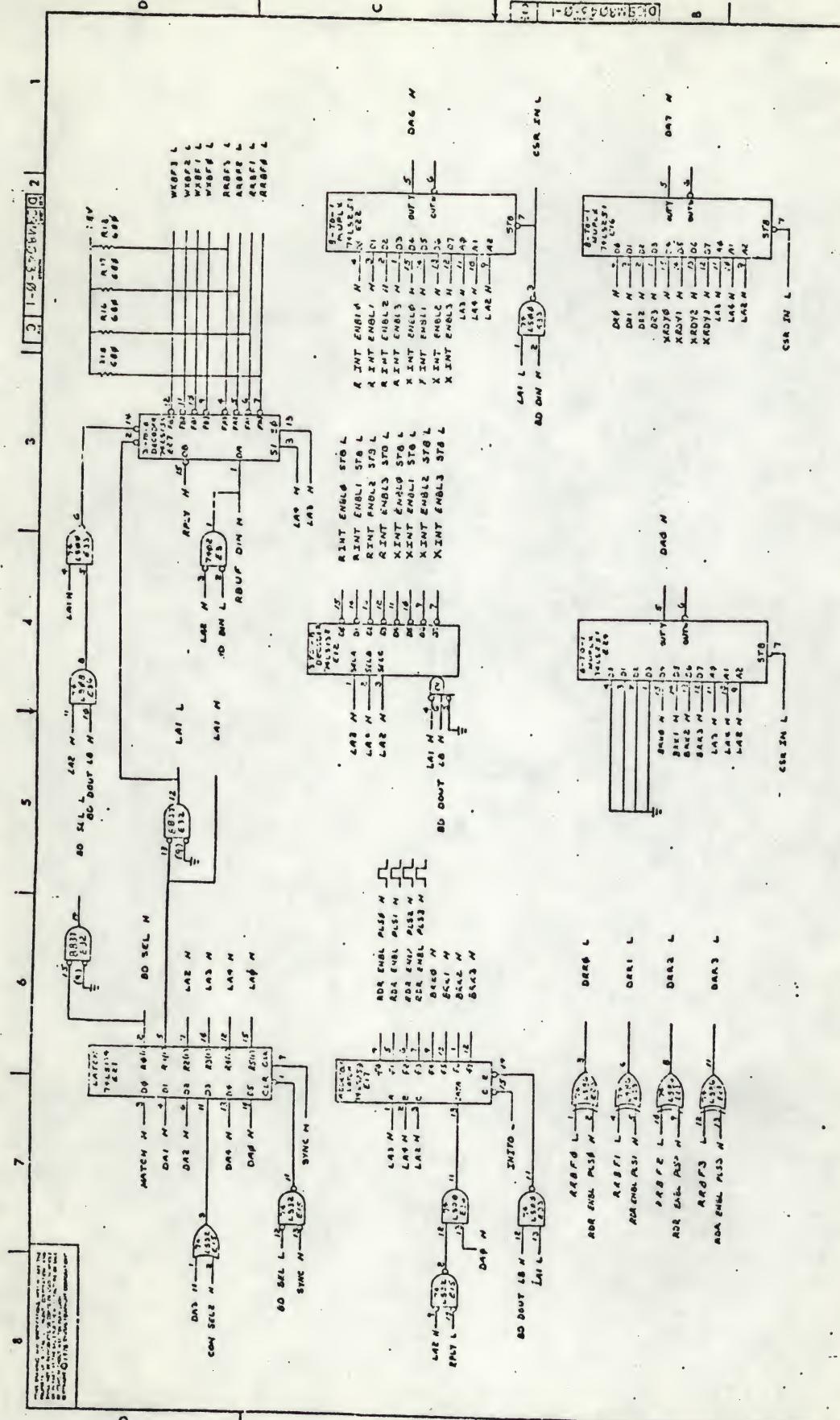




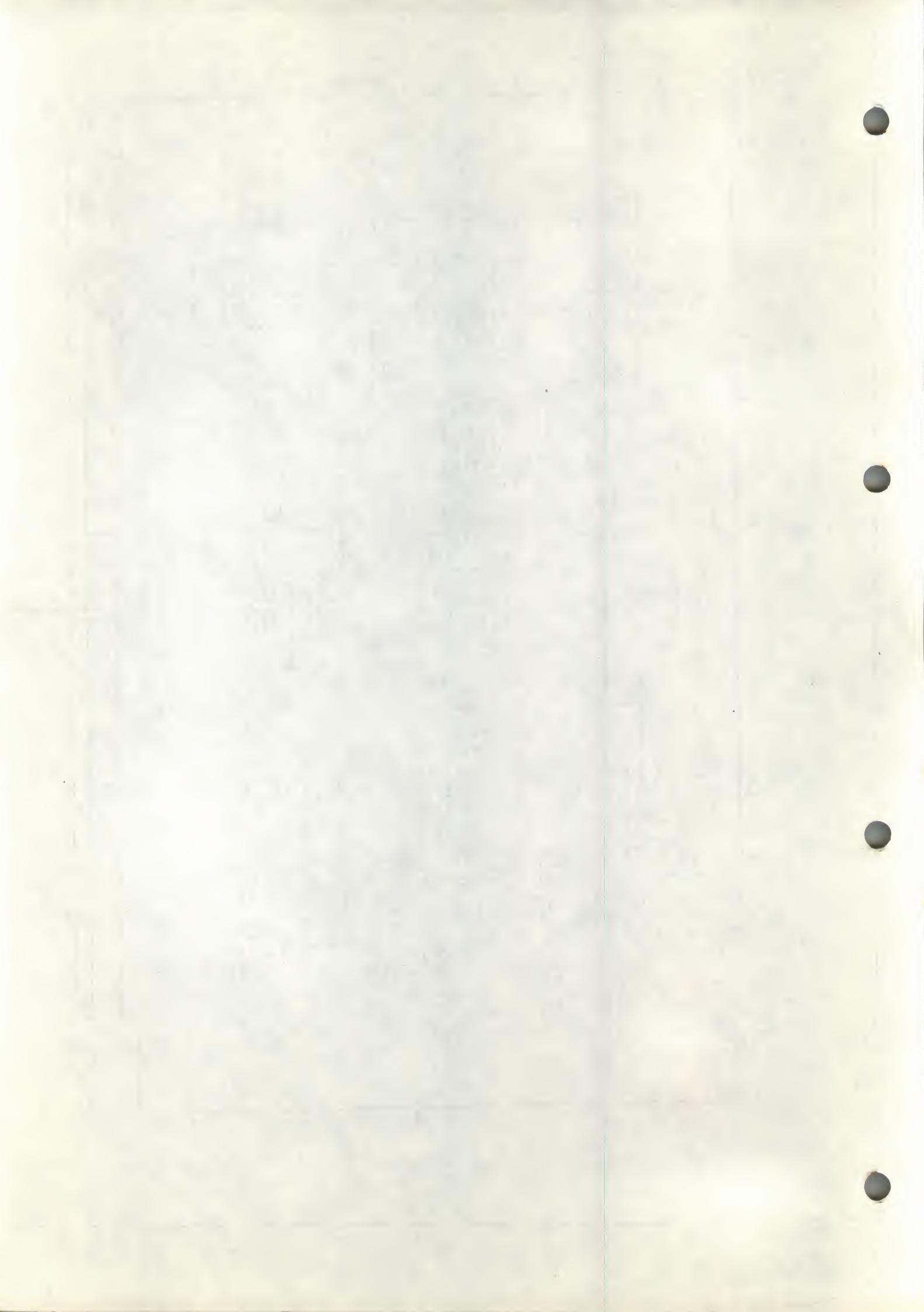


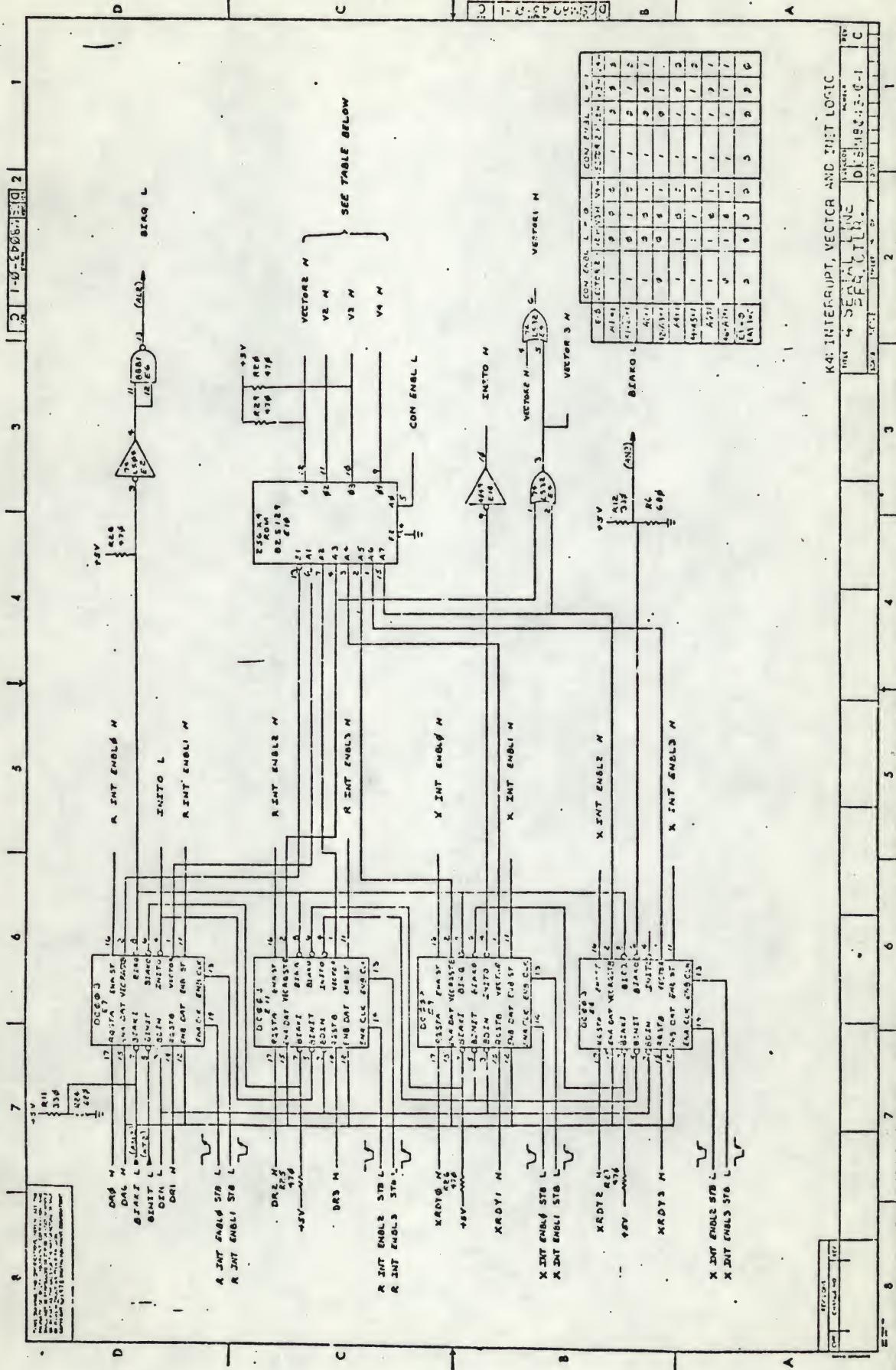


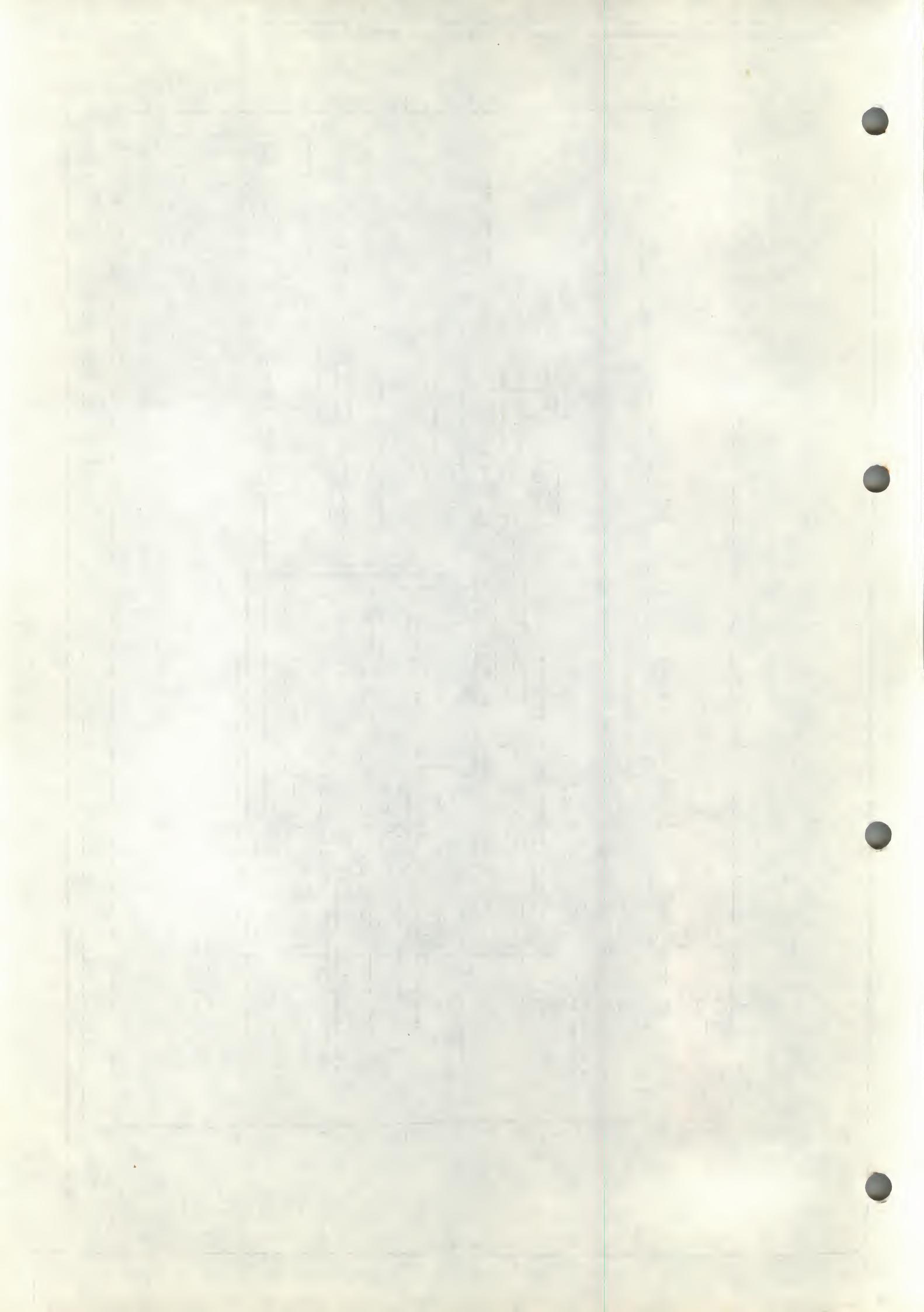




K3: ADDRESS MATCH AND SUCCESS LOGIC

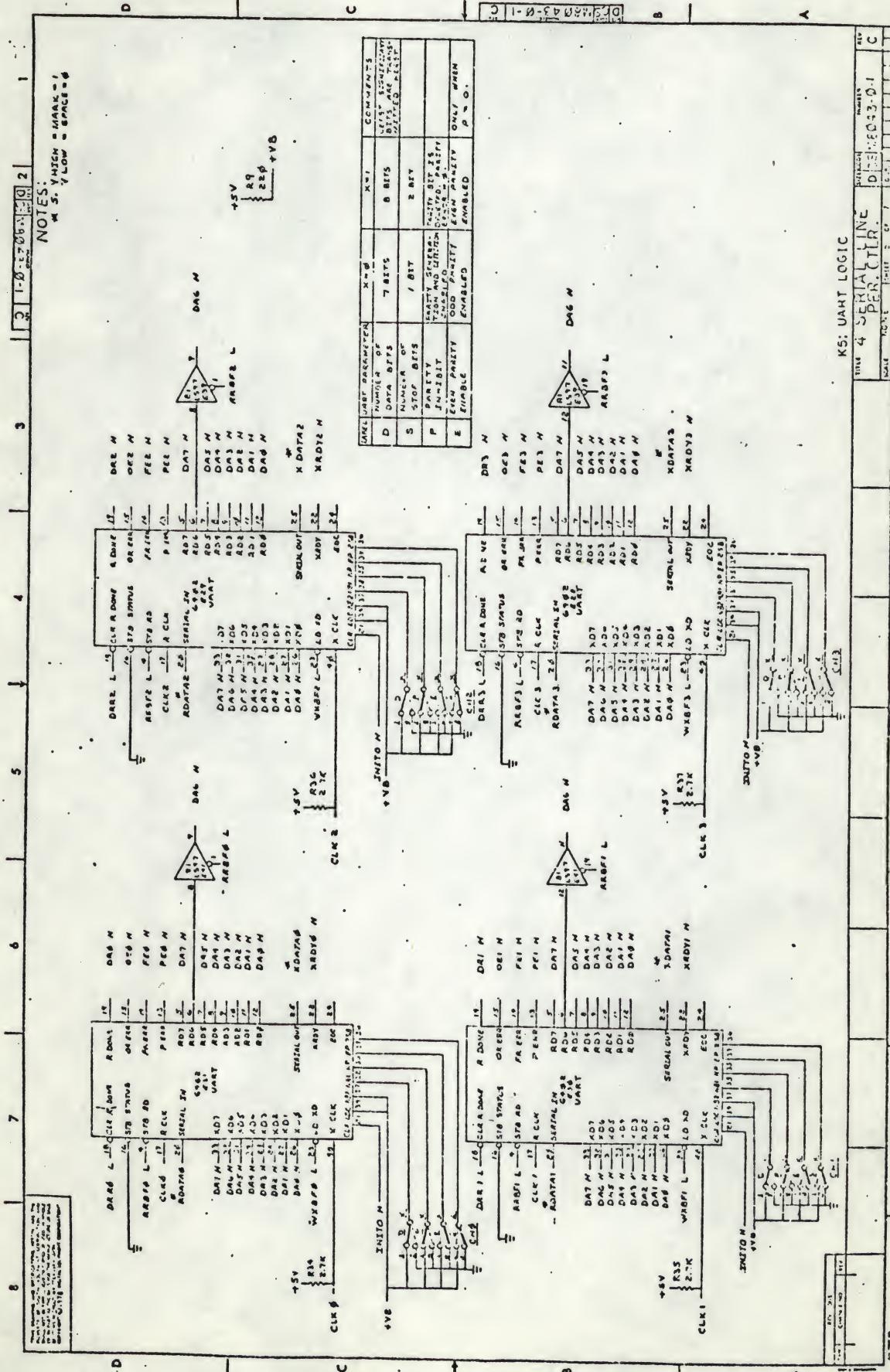


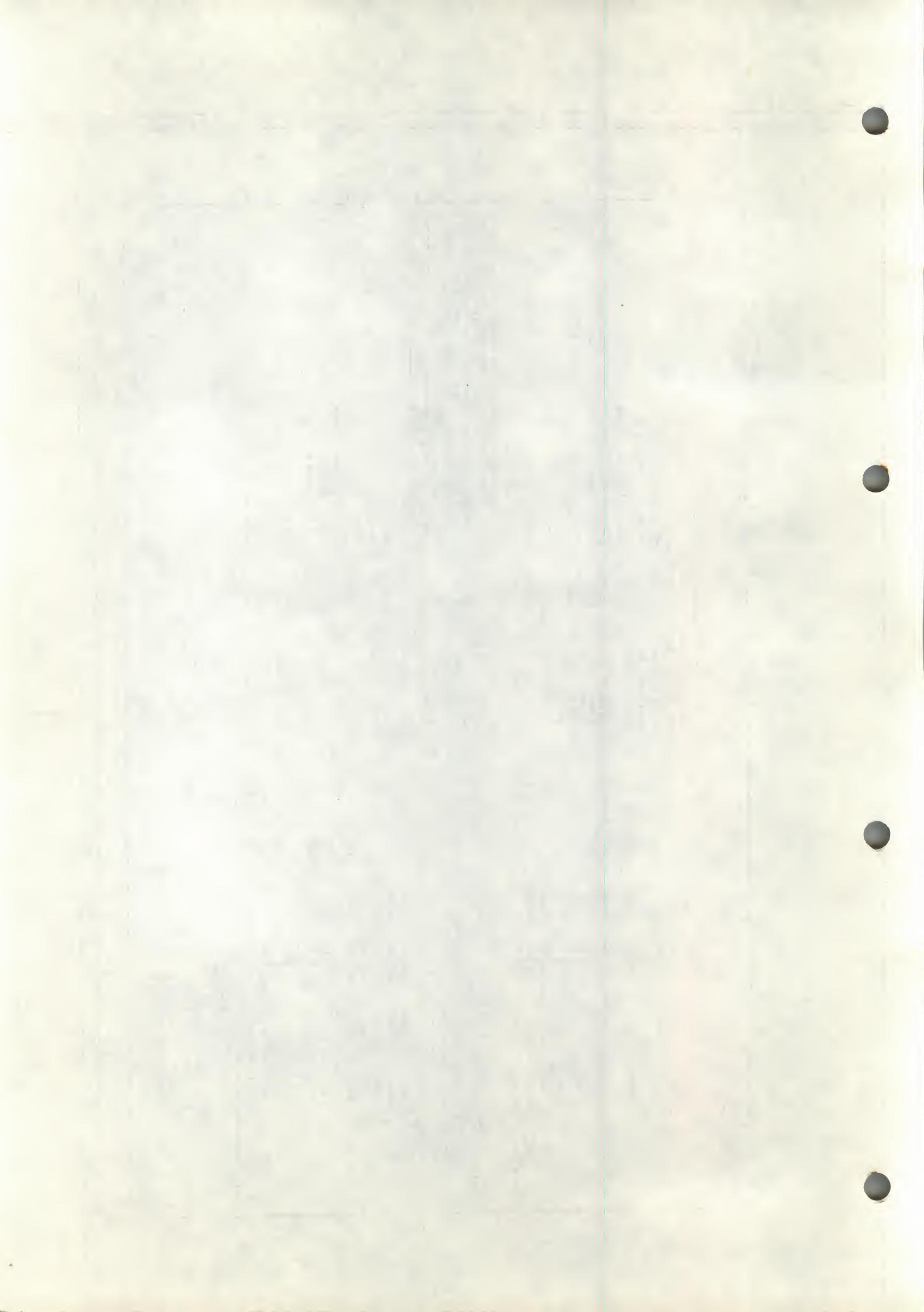




NOTES:  
21  
66-2200  
M. S. MUSC

三



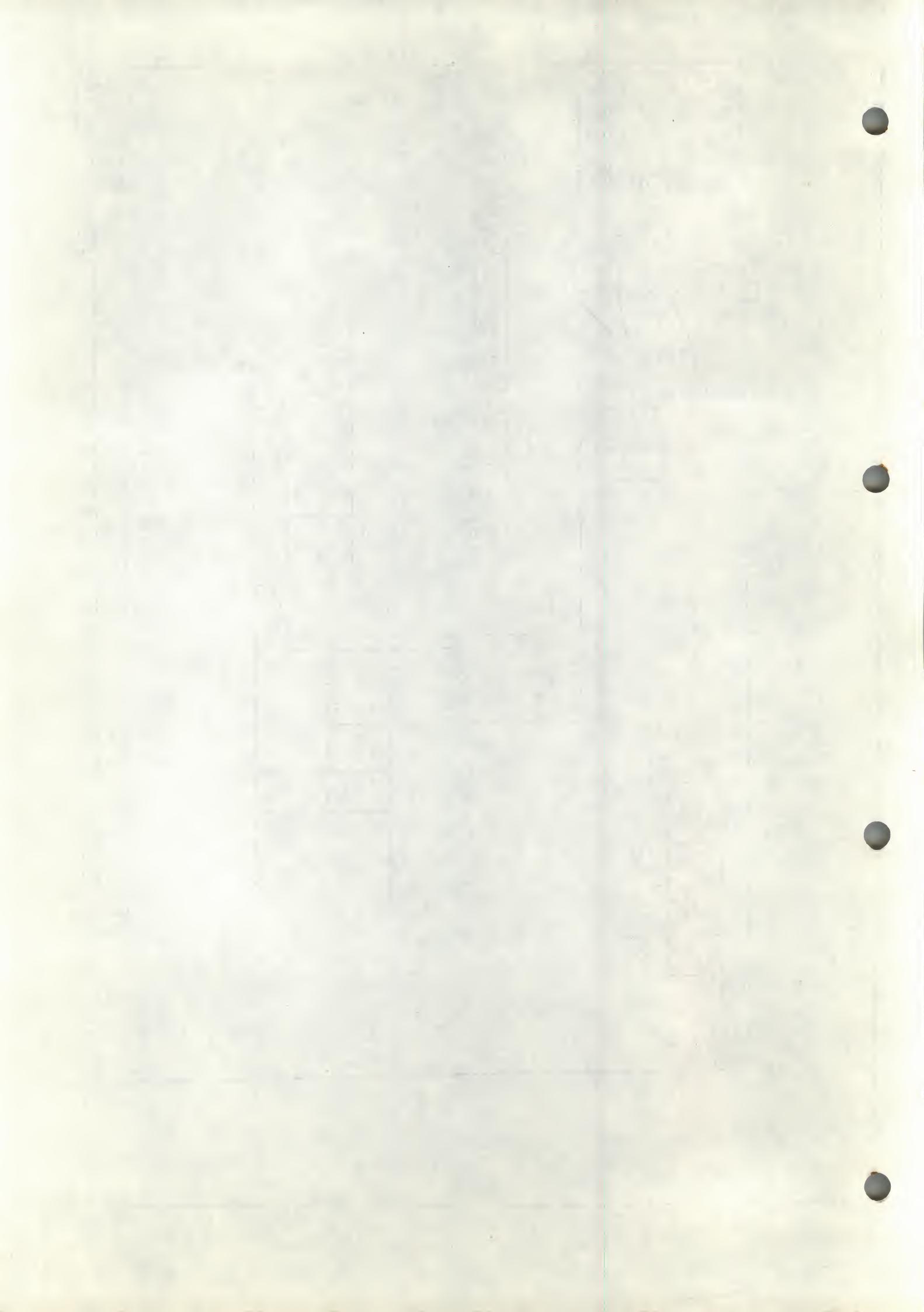


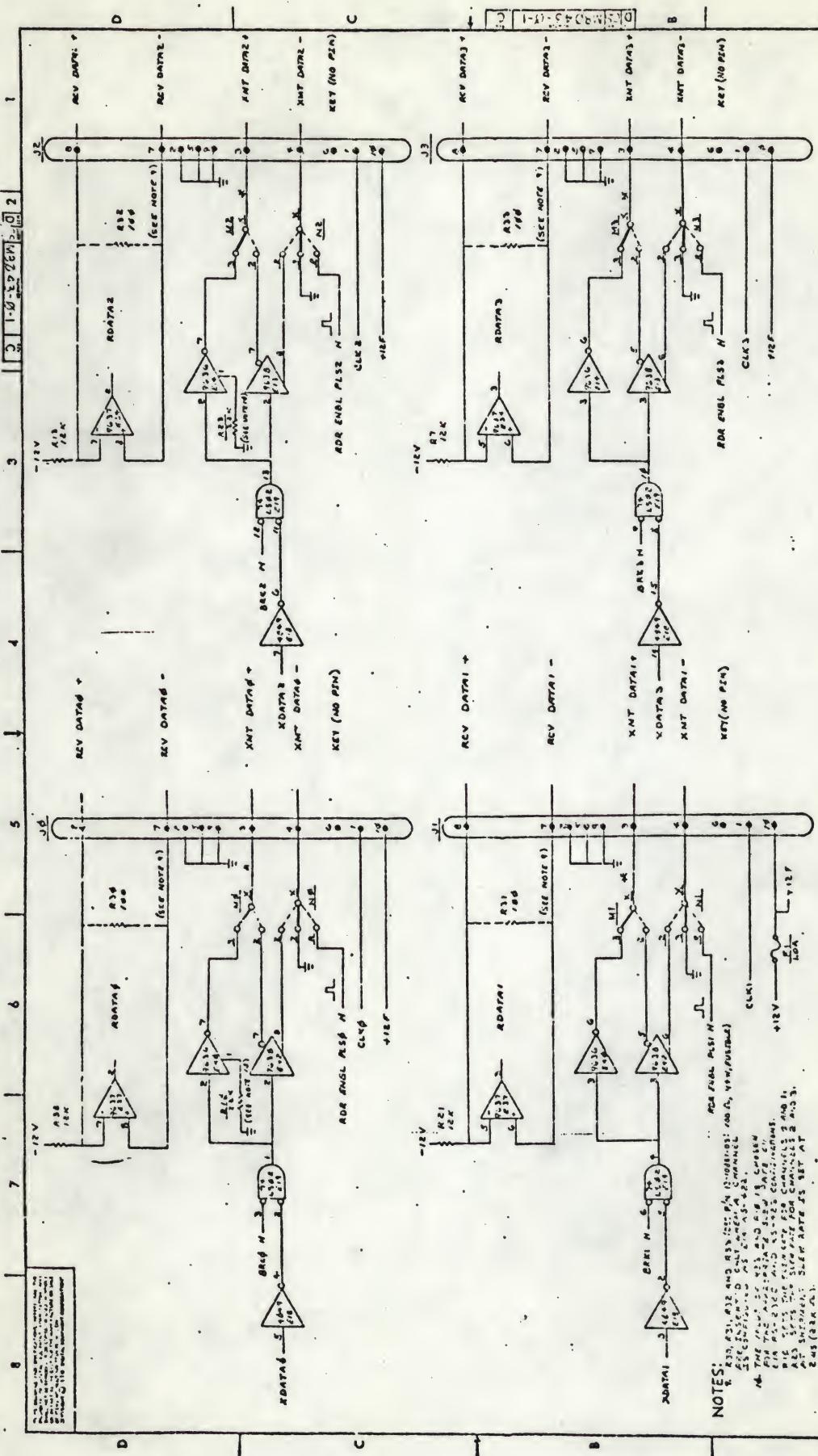
**NOTE:** Since 3 are also required  
6 JUMPS ARE REQUIRED  
7 JUMPS ARE REQUIRED FOR  
ALL TESTS ONLY.

**COUNTER**  
74133  
d15 G 15204  
d14 5 15205  
d13 6 15206  
d12 7 15207  
d11 8 15208  
d10 9 15209  
d9 10 15210  
d8 11 15211  
d7 12 15212  
d6 13 15213  
d5 14 15214  
d4 15 15215  
d3 16 15216  
d2 17 15217  
d1 18 15218  
d0 19 15219  
d15 20 15220  
d14 21 15221  
d13 22 15222  
d12 23 15223  
d11 24 15224  
d10 25 15225  
d9 26 15226  
d8 27 15227  
d7 28 15228  
d6 29 15229  
d5 30 15230  
d4 31 15231  
d3 32 15232  
d2 33 15233  
d1 34 15234  
d0 35 15235  
d15 36 15236  
d14 37 15237  
d13 38 15238  
d12 39 15239  
d11 40 15240  
d10 41 15241  
d9 42 15242  
d8 43 15243  
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$\frac{C_{11}}{C_{11} - C_{12}}$	$\frac{C_{12}}{C_{11} - C_{12}}$	$\frac{C_{11}}{C_{11} + C_{12}}$	$\frac{C_{12}}{C_{11} + C_{12}}$
$\frac{C_{11}}{C_{11} - C_{12}}$	$\frac{C_{12}}{C_{11} - C_{12}}$	$\frac{C_{11}}{C_{11} + C_{12}}$	$\frac{C_{12}}{C_{11} + C_{12}}$
$\frac{C_{11}}{C_{11} - C_{12}}$	$\frac{C_{12}}{C_{11} - C_{12}}$	$\frac{C_{11}}{C_{11} + C_{12}}$	$\frac{C_{12}}{C_{11} + C_{12}}$
$\frac{C_{11}}{C_{11} - C_{12}}$	$\frac{C_{12}}{C_{11} - C_{12}}$	$\frac{C_{11}}{C_{11} + C_{12}}$	$\frac{C_{12}}{C_{11} + C_{12}}$
$\frac{C_{11}}{C_{11} - C_{12}}$	$\frac{C_{12}}{C_{11} - C_{12}}$	$\frac{C_{11}}{C_{11} + C_{12}}$	$\frac{C_{12}}{C_{11} + C_{12}}$

K6: PWR DIST, BAUD RATE GEN & -INV CIRCUITRY  
 INPUT + SERV CT LINE DCS MODE: C-1  
 INPUT - SERV CT LINE DCS MODE: C-0





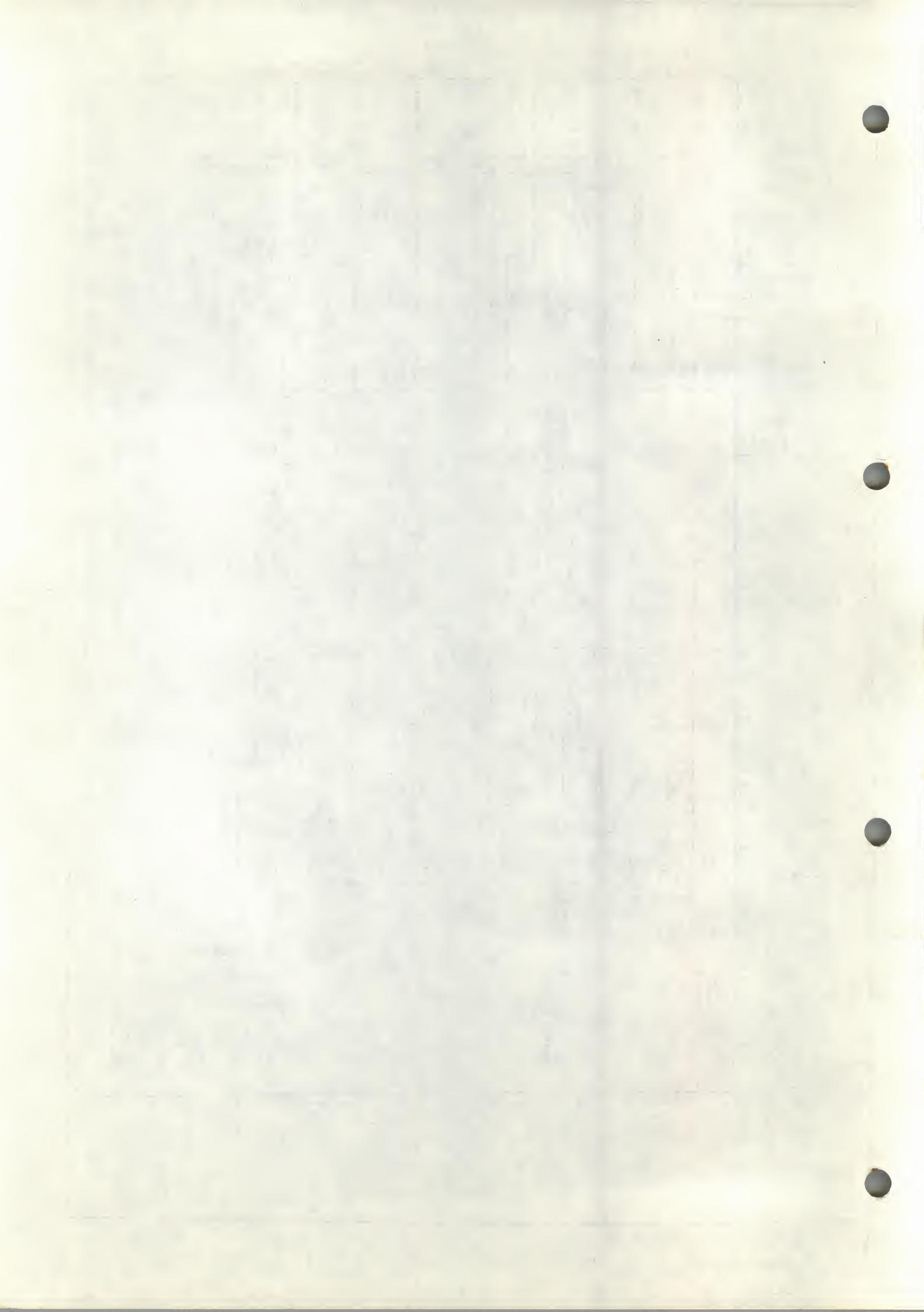
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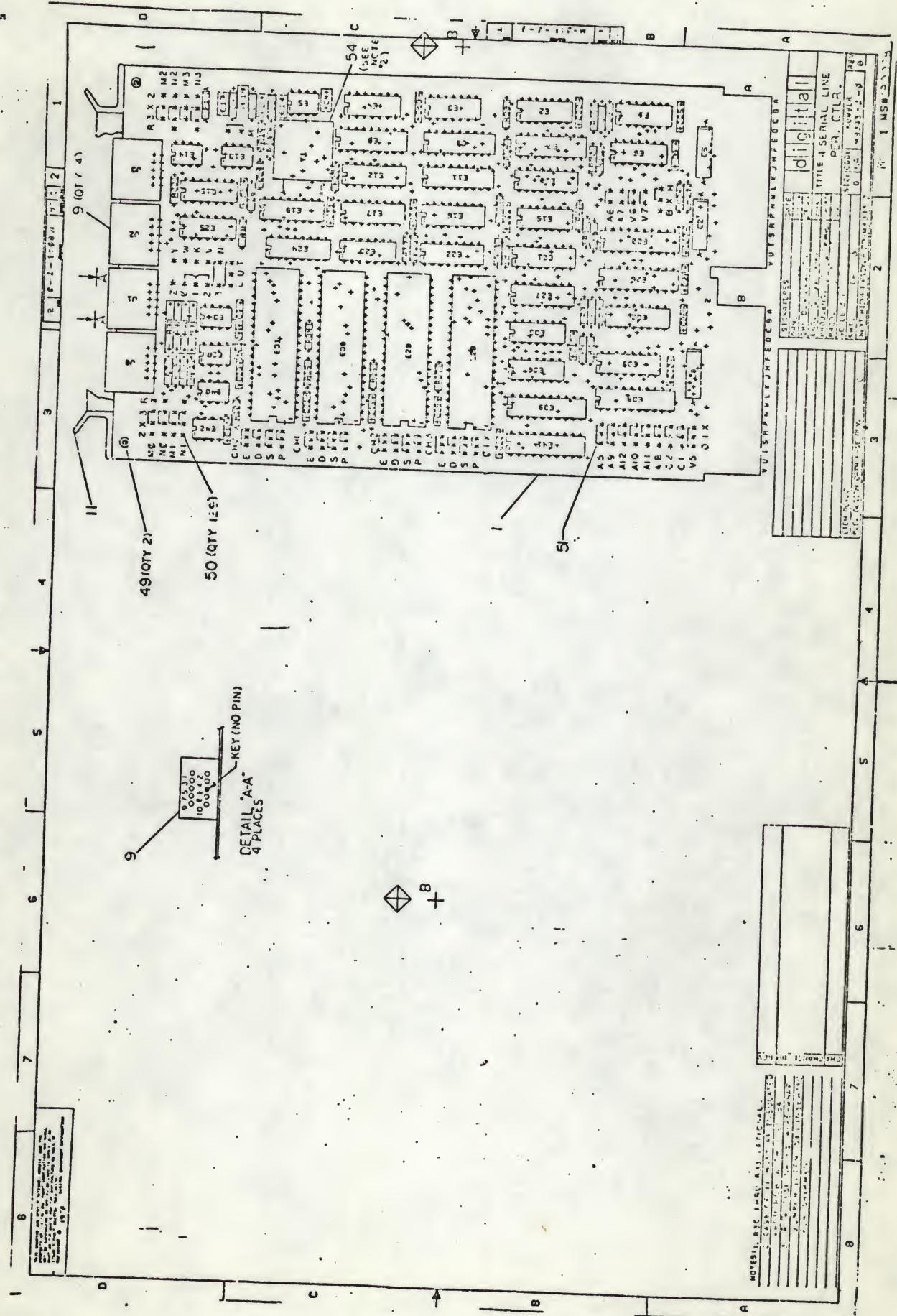
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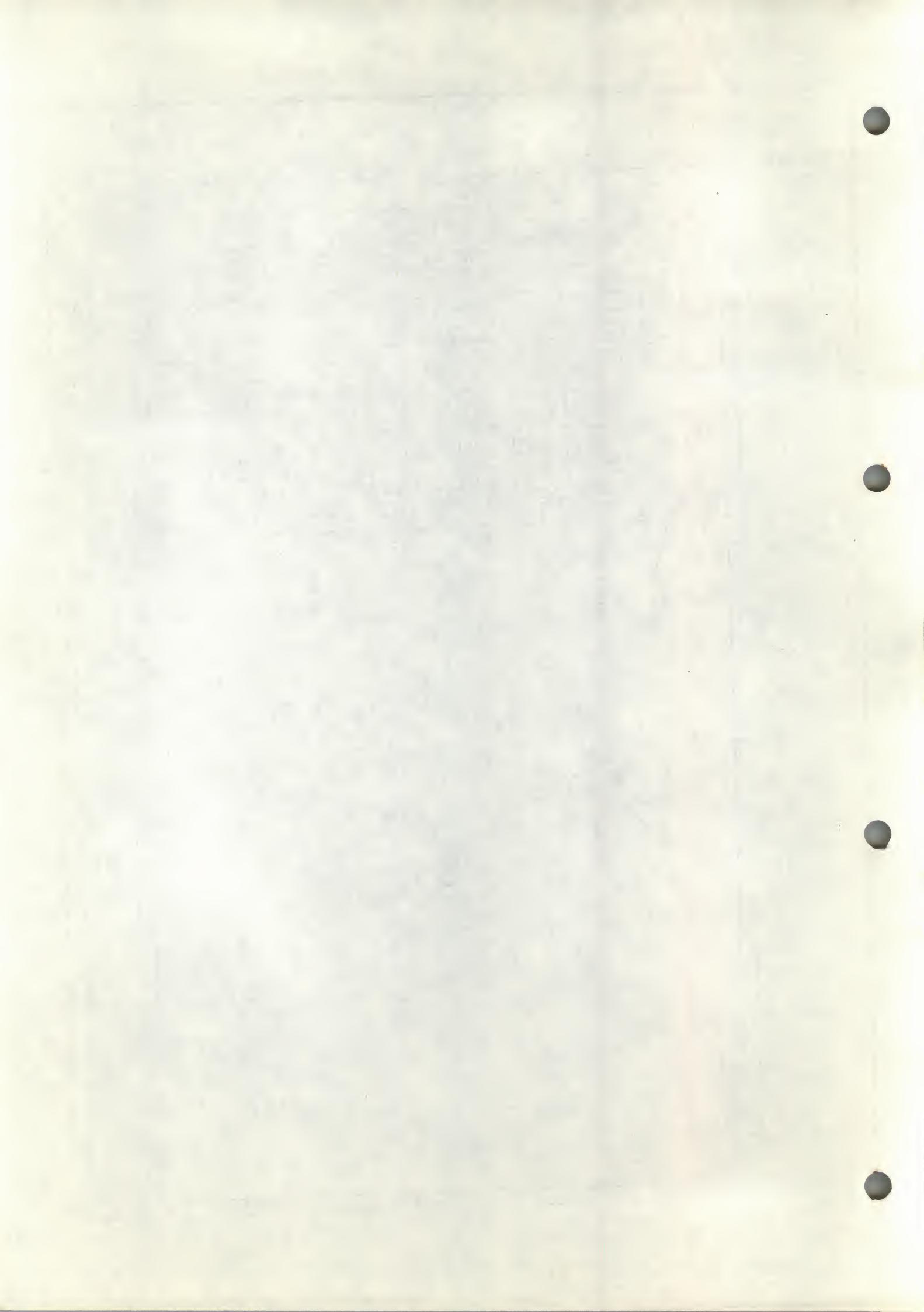
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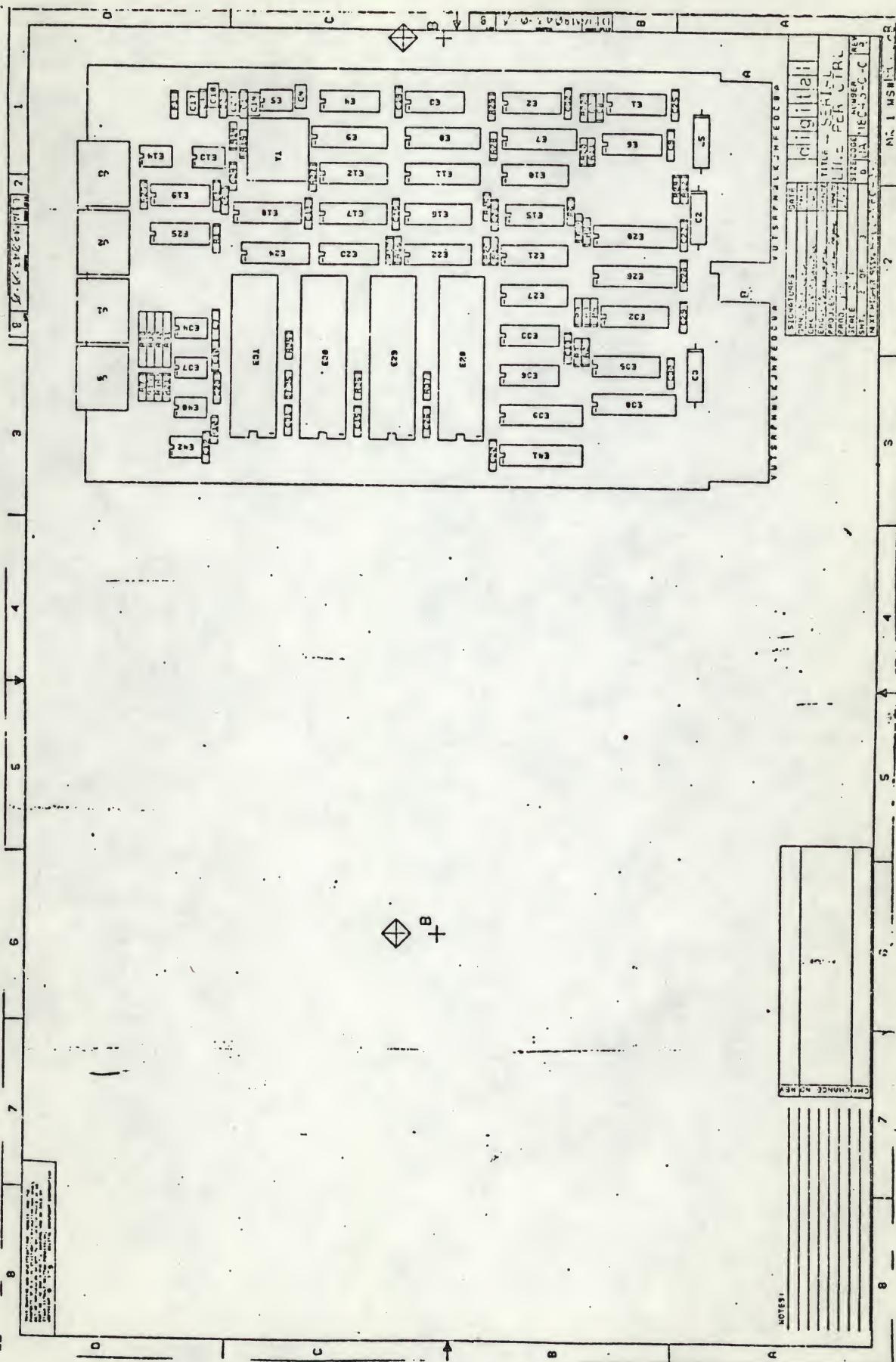
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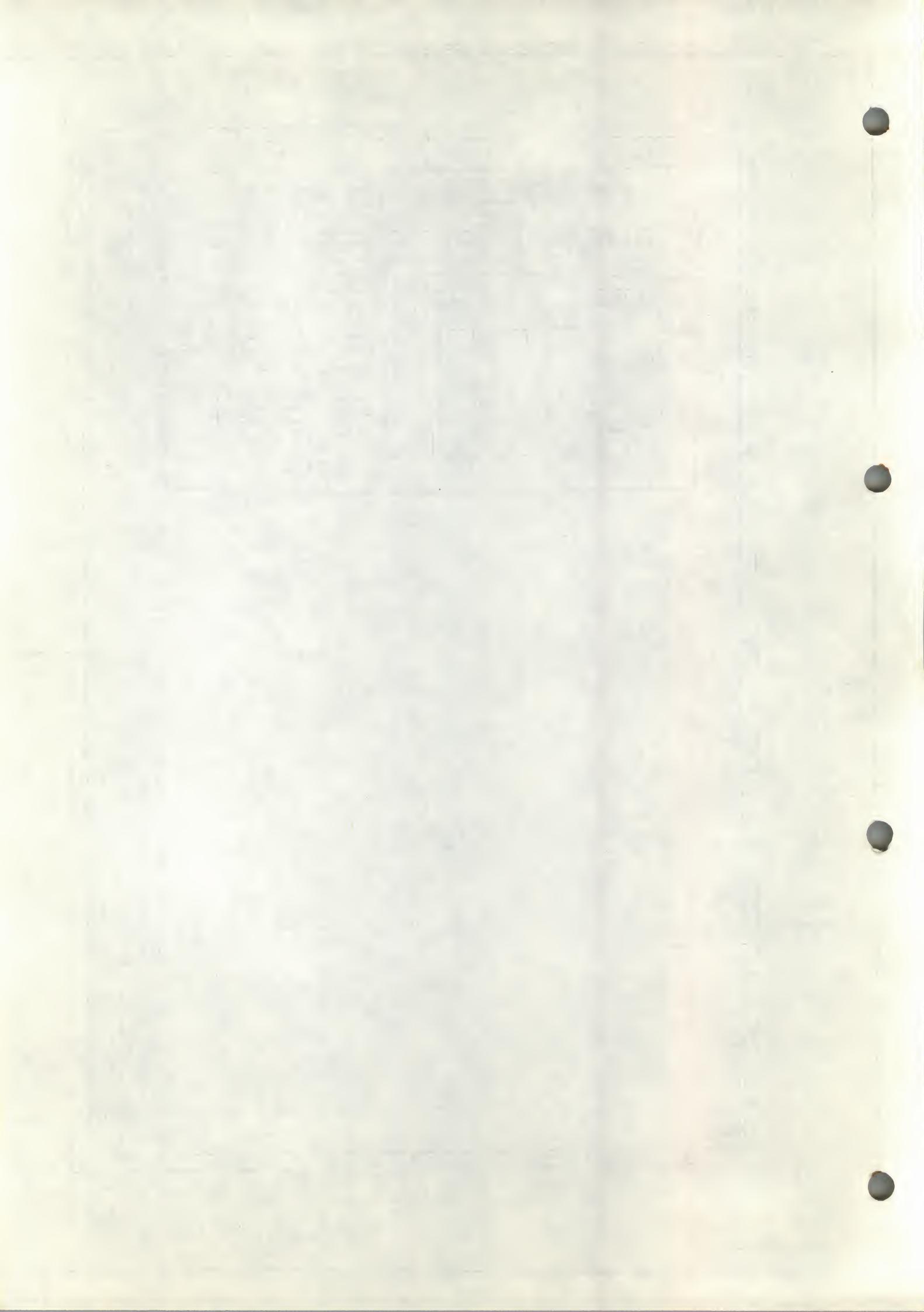
RE: LINE 2000/2001/2002  
LINE 2002  
PFCR, CTR, PFCR  
SOME NOTES  
DATE 1/1/01  
ENV



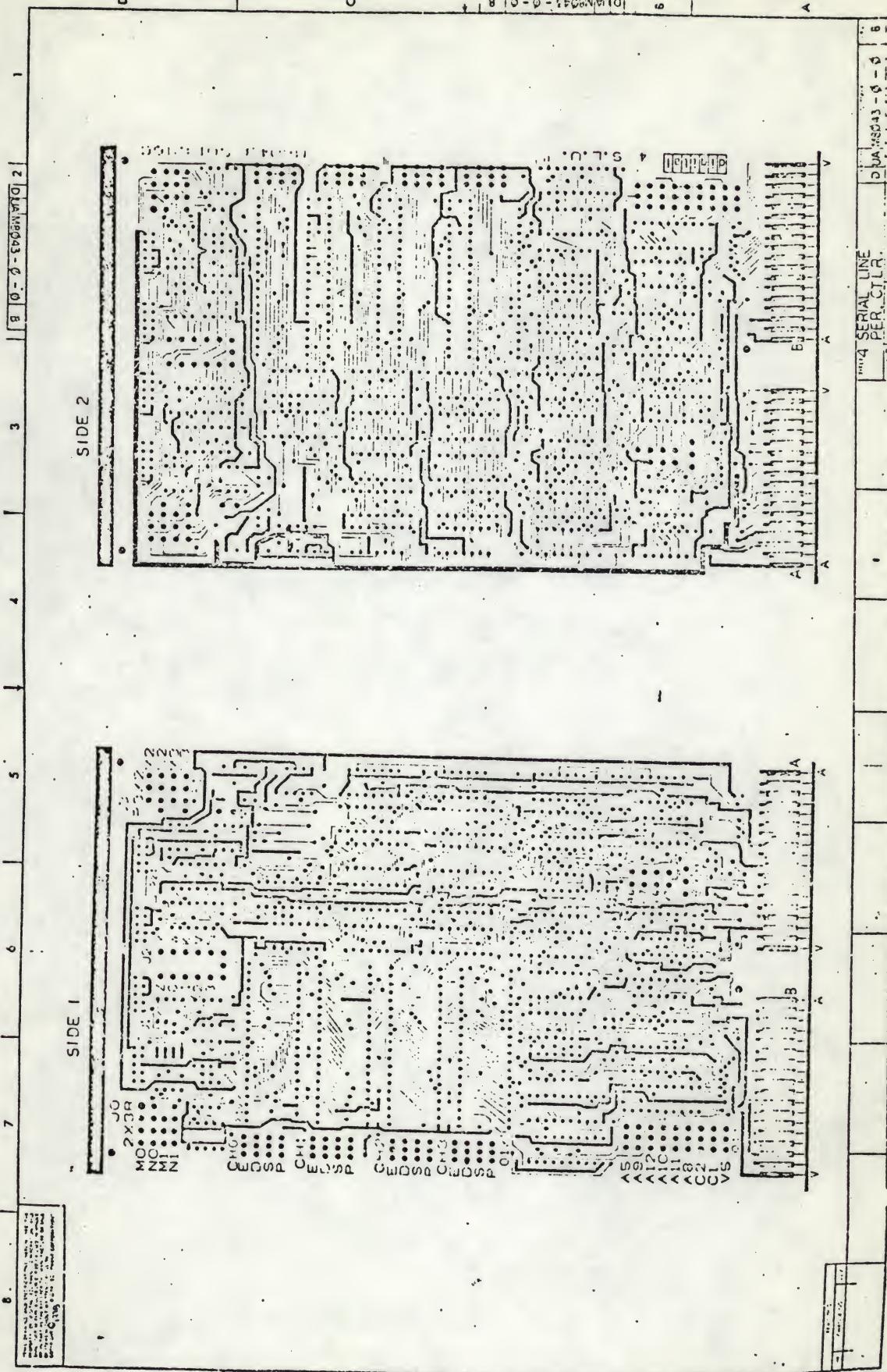


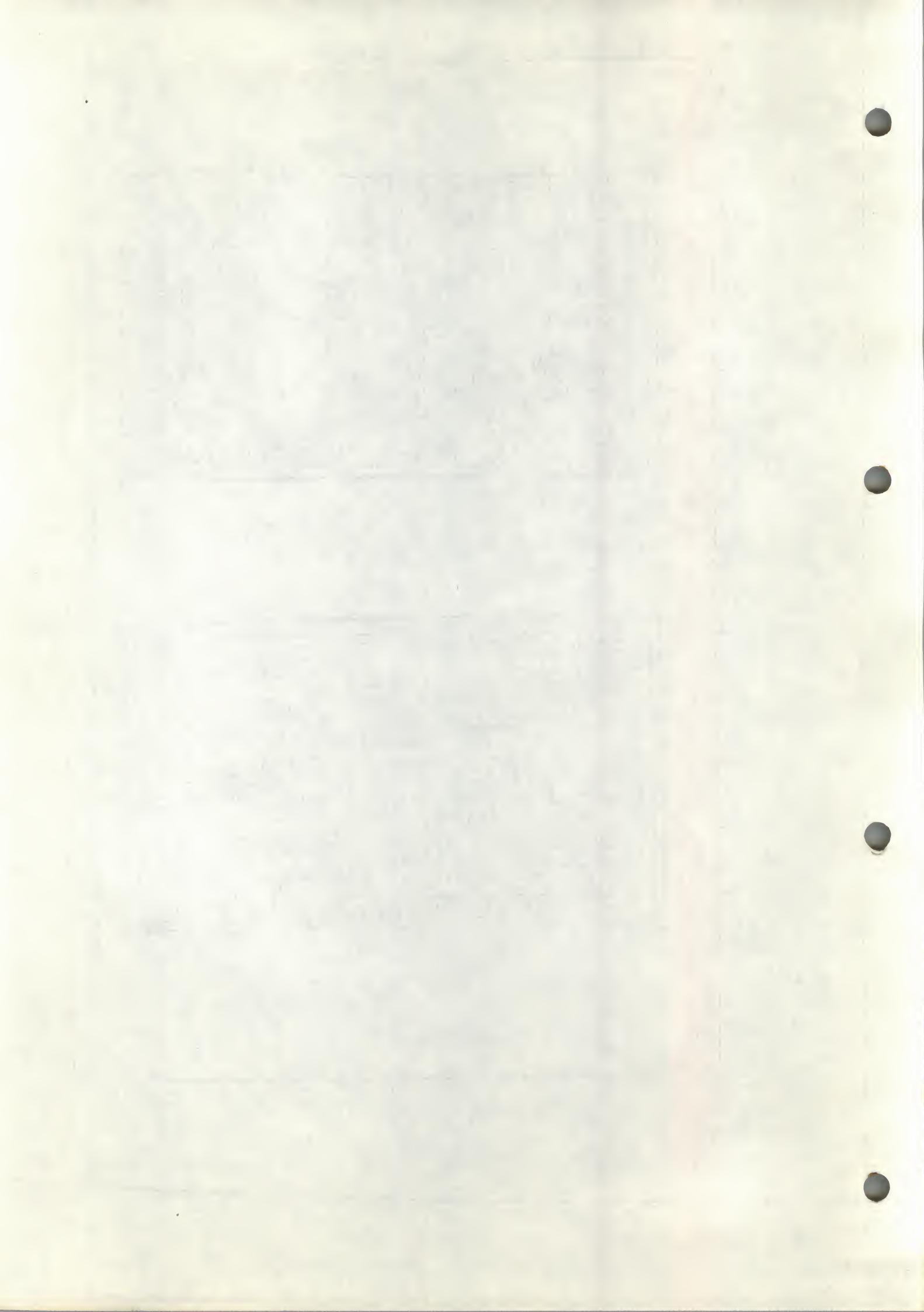




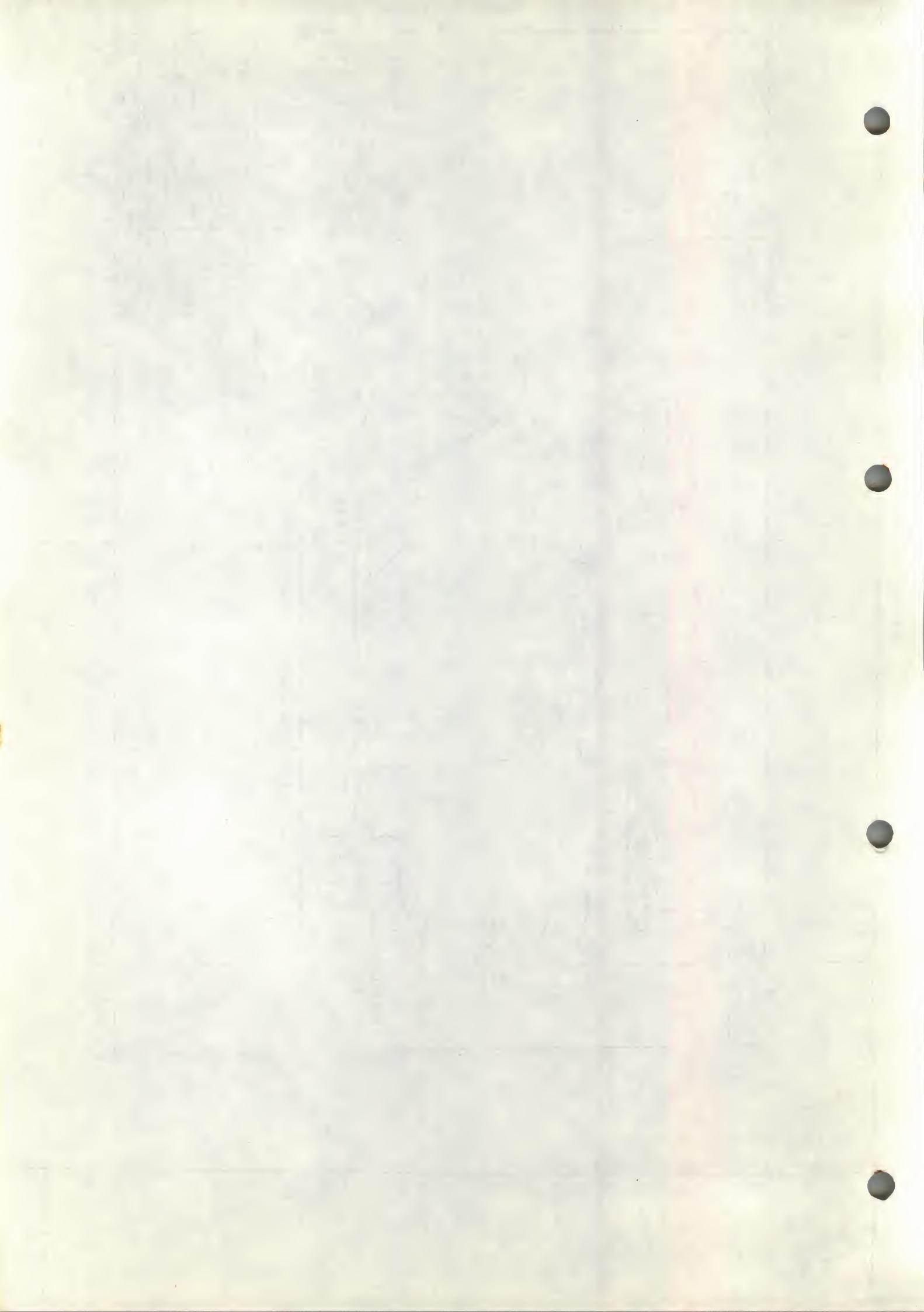


800-0-ECOMNTO

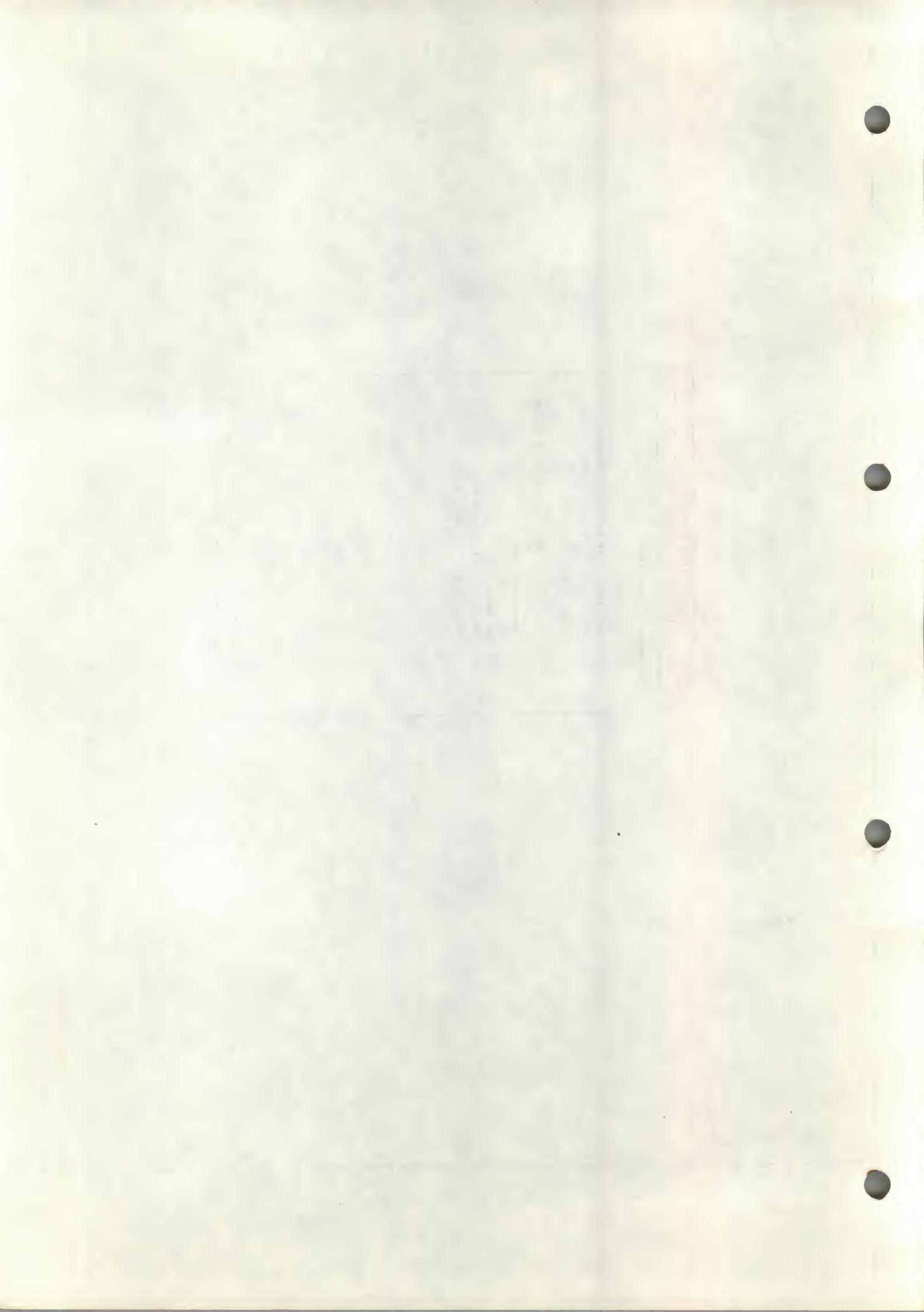








ENGINEERING SPECIFICATION		CONTINUATION SHEET	
TITLE		REV F ENGINEERING SPECIFICATION	
<b>16.0 ENVIRONMENTAL REQUIREMENTS</b>			
<b>16.1 Ambient Temp</b>			
Operating	50°C to 60°C (110°F to 140°F)		
Non-Operating	-40°C to 80°C (-40°F to 176°F)		
<b>16.2 Humidity</b>			
Operating	10% to 95%, Max wet bulb 32°C (90°F) and Min dew point 20°C (68°F)		
Non-Operating	5% to 95%		
<b>16.3 Altitude</b>			
Operating	2.4 km (8,000 ft)		
Non-Operating	9.1 km (30,000 ft)		
SHEET NO. <u>25</u> OF <u>25</u>		REV <u>F</u>	
GSA FORM 1010-1000, 10-64		NUMBER <u>10117</u>	

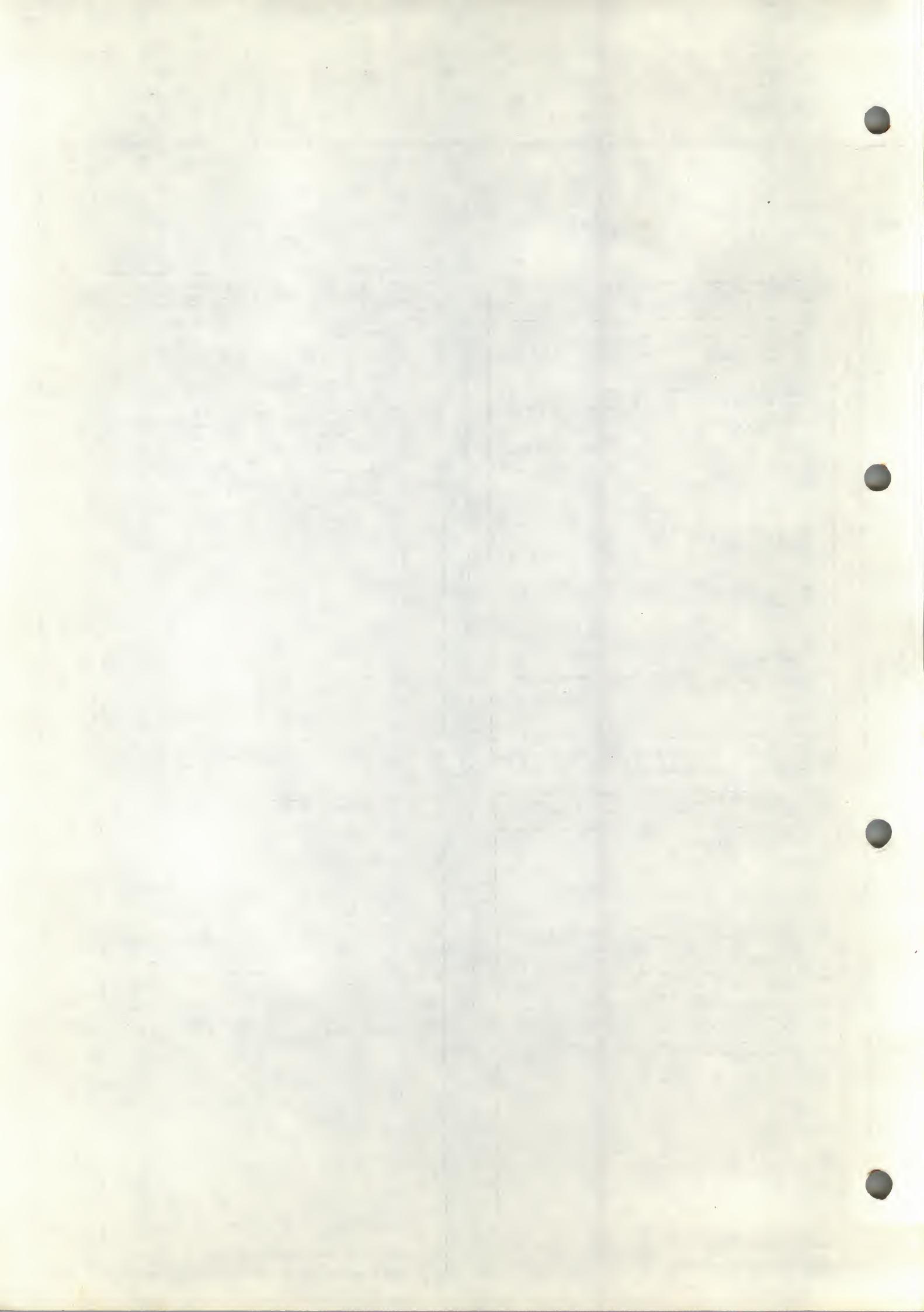


ENGINEERING SPECIFICATION				CONTINUATION SHEET
TITLE DLVII-F ENGINEERING SPECIFICATION				
<p>Contains a crystal oscillator which is connected to a dual baud rate generator which provides appropriate clock signals to the UART. A separate clock is available for the transmitter for split speed operation.</p> <p><b>8.2.7 -12V Charge Pump</b> This circuit provides the -12 volts needed by the UART, the driver (latch) and the PDP RUN current loop. The maximum current supplied by this -12V charge pump is 40mA.</p> <p><b>8.2.8 Reader Run Circuit</b> The Reader Run Circuit is used to advance the paper tape reader in the DDC modified TTY units. This is performed by setting bit 6 of the RCSR to a 1. The Reader Run Circuit then will advance the paper tape one position and serial data will start to be received from the TTY. The start bit of this serial data is used by the Reader Run Circuit to automatically reset the internal bit # flip-flop.</p> <p><b>8.2.9 20mA Interface</b> This circuit converts TTL level serial data to standard 20mA Current Loop Serial Data and vice versa. This circuit allows direct connection to DDC's LA36, VT32, etc. and to the DDC modified TTY, both the receiver and transmitter may operate in either the active or passive mode.</p> <p><b>8.2.10 EIA Interface</b> This interface provides the proper level converters for serial data for connection to EIA terminals such as the VT56 or the model 37 TTY through a null modem. (See EIA Standard RS-232-C).</p> <p>This circuit strips EIA Data Terminal Ready, EIA Request to Send signals to the CPU position, thus making it possible for the parallel to interface to the Model 1072 datasets which will automatically assert incoming calls. This type of connection, however, does not provide for properly terminating the call.</p> <p>EIA FORCE BUSY signal is also strapped ON for use with the model 1072 modems.</p>				
SIZE	CODE	NUMBER	REV	
A	SP	DLVII-F.2		
DCC FORM NO. EN-01022 (MAY 1970)				
SHEET 25 OF 25				

ENGINEERING SPECIFICATION				CONTINUATION SHEET
TITLE DLVII-F ENGINEERING SPECIFICATION				
<p><b>9.0 TIMING DIAGRAMS</b> In the following timing diagrams, signals are referenced from the output of the bus receiver to the input of the bus driver.</p> <p><b>9.1 DAT Bus Cycle Timing</b></p> <p>Detailed description: The diagram shows six signals over time. R-DAL has a pulse labeled 'R-ADDR'. P-SYNC has a pulse labeled 'P-SYNC'. R-DOUT has a pulse labeled 'MSB-MIN' and 'LSB-MAX'. T-RPLY has a pulse labeled 'T-RPLY'. P-NBT has a pulse labeled 'ASSERTION FOR LS1C'. R-BST has a pulse labeled 'LS1C'.</p>				
SIZE	CODE	NUMBER	REV	
A	SP	DLVII-F.2		
DCC FORM NO. EN-01022 (MAY 1970)				
SHEET 25 OF 25				

ENGINEERING SPECIFICATION				CONTINUATION SHEET
TITLE DLVII-F				
<p><b>9.2 DATA OR DATCB Bus Cycle</b></p> <p>Detailed description: The diagram shows six signals over time. R-DAL has a pulse labeled 'R-ADDR'. P-SYNC has a pulse labeled 'P-SYNC'. R-DOUT has a pulse labeled 'MSB-MIN' and 'LSB-MAX'. T-RPLY has a pulse labeled 'T-RPLY'. P-NBT has a pulse labeled 'ASSERTION FOR LS1C'. R-BST has a pulse labeled 'LS1C'.</p>				
SIZE	CODE	NUMBER	REV	
A	SP	DLVII-F.2		
DCC FORM NO. EN-01022 (MAY 1970)				
SHEET 25 OF 25				

ENGINEERING SPECIFICATION				CONTINUATION SHEET
TITLE DLVII-F ENGINEERING SPECIFICATION				
<p><b>9.3 Interrupt Timing</b></p> <p>Detailed description: The diagram shows five signals over time. T-IRO has a pulse labeled 'I-F1 MIN' and 'I-F2 MAX'. R-DIN has a pulse labeled 'I-F1 MIN' and 'I-F2 MAX'. R-JAKI has a pulse labeled 'JAKI'. T-RPLY has a pulse labeled 'T-RPLY'. T-DAL has a pulse labeled 'VECTOR' and 'I-F1 MAX'.</p>				
SIZE	CODE	NUMBER	REV	
A	SP	DLVII-F.2		
DCC FORM NO. EN-01022 (MAY 1970)				
SHEET 25 OF 25				



ENGINEERING SPECIFICATION		CONTINUATION SHEET													
TITLE		DEVII-F ENGINEERING SPECIFICATION													
<b>Bit</b>	<b>Func.</b>	<b>Meaning and Operation</b>													
1	RESERVED	Not applicable. Read as 0s.													
0	BREAK	When set, transmits a continuous space to the external device.													
Read/write bit is cleared by INIT.		7.1.4 Transmitter Buffer Register													
RESERVED		TRANSMITTER DATA BUFFER													
35	14	13	12	31	16	9	8	7	6	5	4	3	2	1	0

FIGURE 5 TRANSMITTER BUFFER REGISTER (TDBF) - BIT ASSIGNMENTS

<b>Bit</b>	<b>Note</b>	<b>Meaning and Operation</b>
15-8	RESERVED	Not applicable. Undefined when read.
7-0	TRANSMITTER DATA BUFFER	Holds the character to be transferred to the external device. If less than eight bits are used, the character must be loaded so that it is right justified into the least significant bits.  Write only bits. Undefined when read.

7.2 Interrupts

The DEVII-F has two interrupt channels: one for the receiver section and one for the transmitter section. These two channels operate independently; however, if simultaneous interrupt requests occur, the receiver has priority.

A transmitter interrupt can occur only if the interrupt enable bit (XMIT INT ENB) in the transmitter status register is set. With XMIT INT Enb set, selecting the transmitter ready (XMIT RDY) bit initiates an interrupt request. When XMIT RDY is set, it indicates that the transmitter buffer is empty and ready to accept another character from the bus for transfer to the external device.

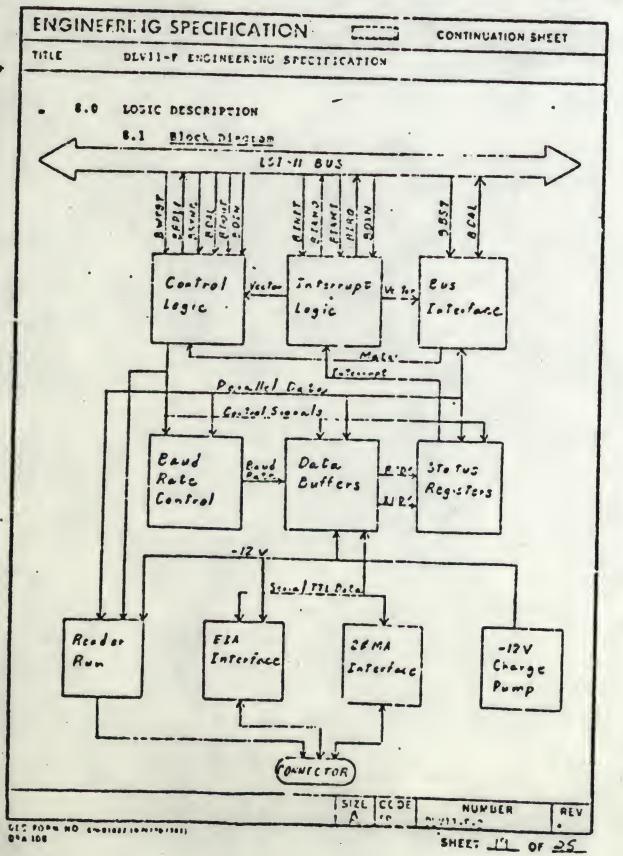
DEC FORM NO. EN-1025 (MAY 1970) 2000  
GSA 108

SHEET 17 OF 25

ENGINEERING SPECIFICATION		CONTINUATION SHEET	
TITLE		DEVII-F ENGINEERING SPECIFICATION	
<p>A receiver data interrupt can occur only if the interrupt enable (RCVR INT ENB) bit in the receiver status register is set. With RCVR INT RDY set, setting the receiver ready (RCVR RDY) bit initiates an interrupt request. When RCVR RDY is set, it indicates that an entire character has been received and is ready for transfer to the bus.</p> <h3>7.3 Timing Considerations</h3> <p>When programming the DEVII-F Asynchronous Line Interface, it is important to consider timing of certain functions in order to use the system in the most efficient manner. Timing considerations for the receiver, transmitter and break generation logic are discussed in the following paragraphs.</p> <h4>7.3.1 Receives</h4> <p>The RCVR DONE flag (bit 7 in the RXSH) (URDF) has assembled a full character. This occurs at the middle of the first data bit. Because the UART is double buffered, data remains valid until the next character is received and assembled. This permits one full character time for servicing the RCVR DONE flag.</p> <h4>7.3.2 Transmitter</h4> <p>The transmitter section of the UART is not start initialized; when the buffer (XBUF) is loaded with the first character from the bus, the flag clears but then sets again within a fraction of a bit time. A second character remains cleared for nearly one full character time.</p> <h4>7.3.3 Break Generation Logic</h4> <p>When the BBREAK bit is set, it causes transmission of a continuous space. Because the XMIT RDY flag controls to function normally, the duration of a break can be timed by the pseudo-transmission of a number of characters. Therefore, because the transmitter section of the UART is double buffered, a null character (all 1s) should precede transmission of the break to insure that the previous character clears the line. In a similar manner, the final pseudo-transmitted character in the break should be a null.</p>			

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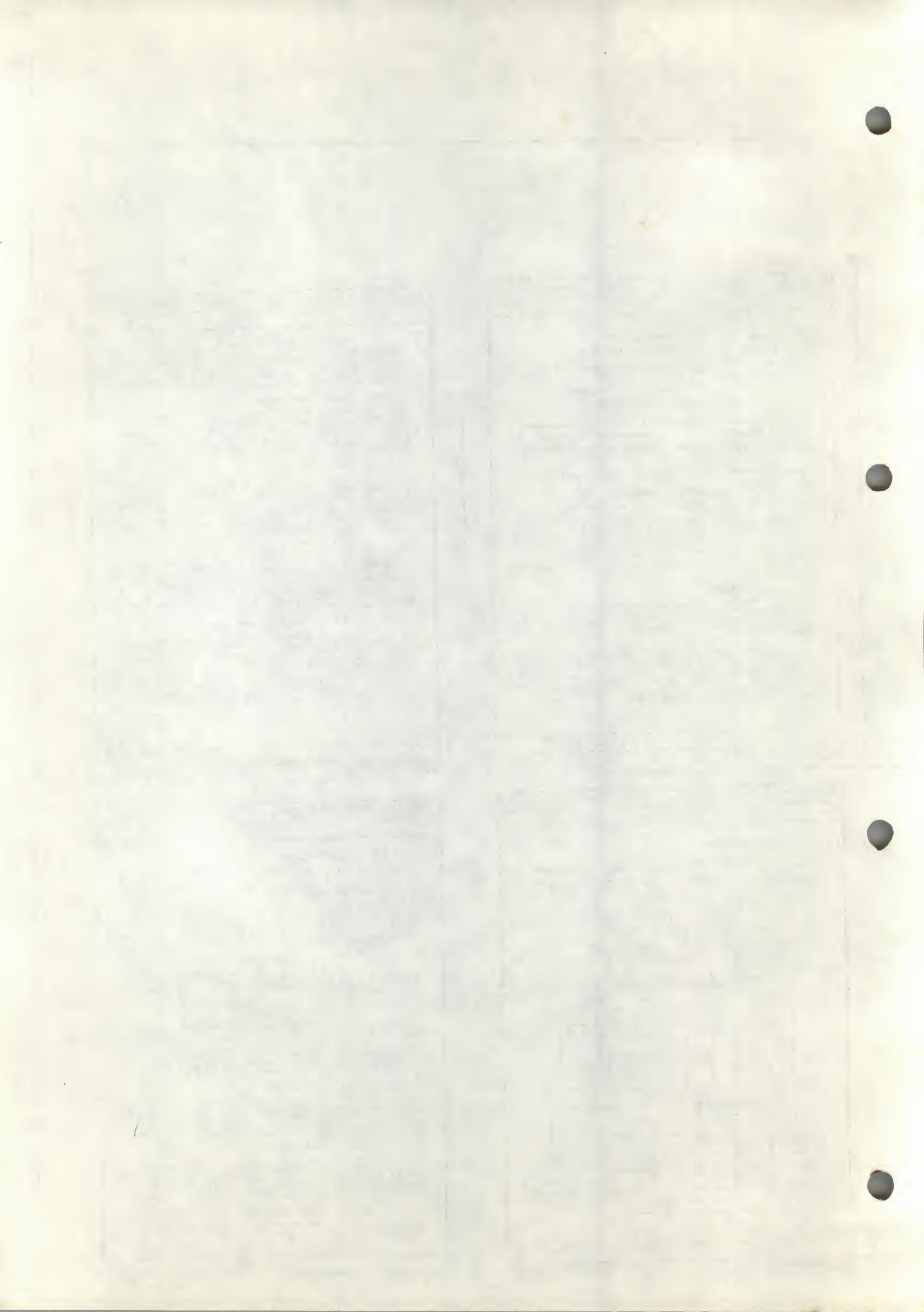
SHEET 18 OF 25



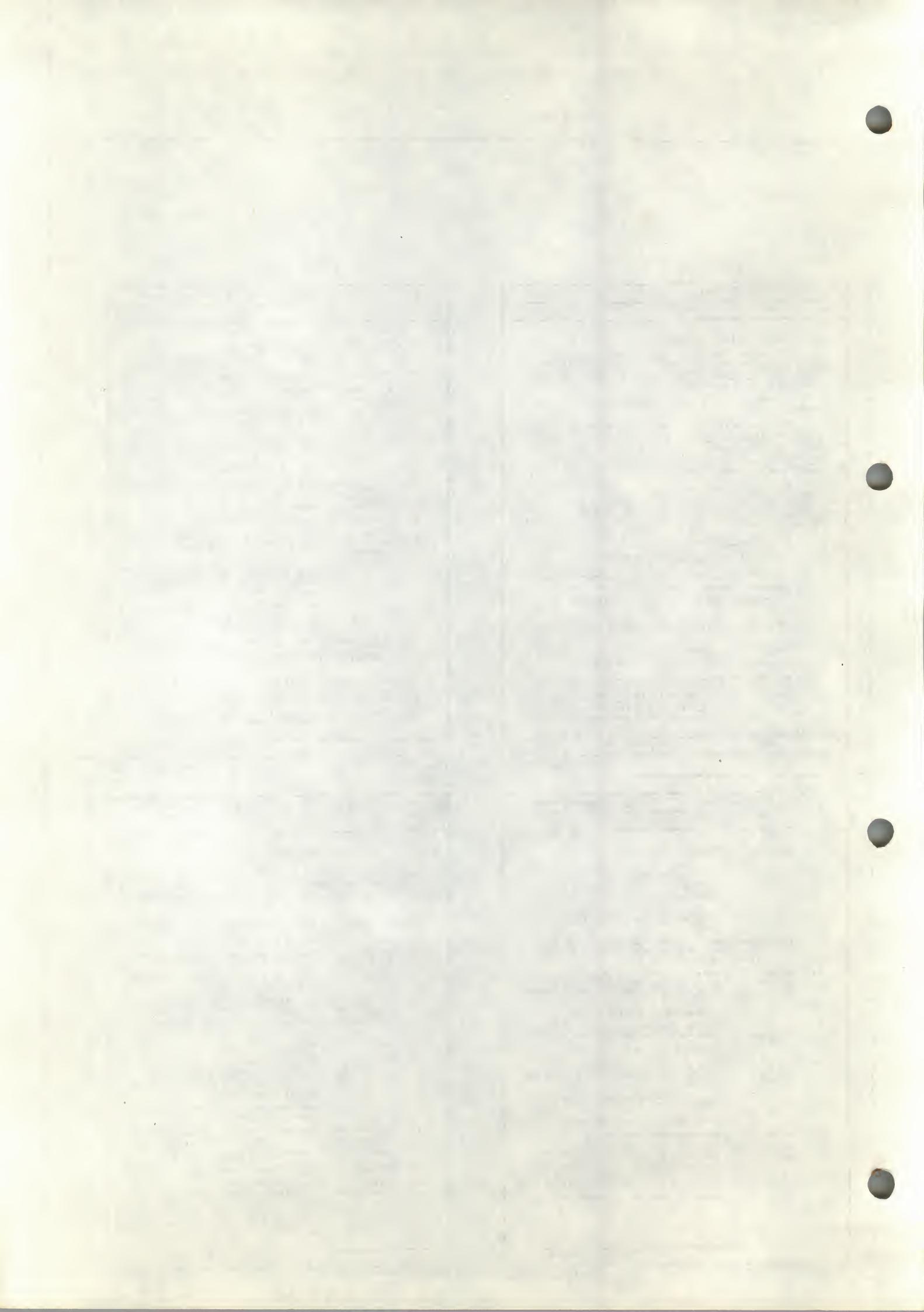
ENGINEERING SPECIFICATION		CONTINUATION SHEET	
TITLE		DEVII-F ENGINEERING SPECIFICATION	
<h3>8.2 Logic Description</h3> <h4>8.2.1 Bus Interface</h4> <p>The bus interface is comprised partly of DC825 transceiver chips. These chips contain bus transceivers that connect the BDAL lines with the internal tri-state bidirectional bus. This chip also provides jumper inputs for address selection and selects a MATCH II open collector output signal when there is an address match. These chips also contain jumper inputs for vector address selection that allow the vector to be asserted on the BDAL lines of the bus.</p> <h4>8.2.2 Interrupt Logic</h4> <p>The interrupt logic provides for two interrupts, A and B, with A having the highest priority. Port A services the receiver interrupts and Port B services the transmitter interrupts.</p> <h4>8.2.3 Control Logic</h4> <p>The major portion of the control logic is provided by the DC824 protocol chip. The protocol chip receives BDIN, BDOUT, BYWC, BTWT and issues BPRIV. It also generates outputs based on the three least significant BDAL lines indicating which of the on-board registers are being addressed. It also indicates which byte or bytes are being operated on and whether the transaction is a DIN or DOUT.</p> <h4>8.2.4 Status Registers</h4> <p>There are two status registers on the module, a receiver status register and a transmitter status register. Information is fed to the flip-flops comprising the status registers via the tri-state DAT bus. Information is read from the registers also through this same DAT bus.</p> <h4>8.2.5 Data Buffers</h4> <p>The data buffers are comprised of a Universal Asynchronous Receiver/Transmitter (UART). The UART accepts parallel data and serializes it with start bits and stop bits for transmitter operations. It also accepts serial data and changes it to parallel form for receiver operations.</p> <h4>8.2.6 Baud Rate Control</h4> <p>The baud rate is jumper selectable or program selectable over the range 50 - 19200 bps. The circuit</p>			

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ENGINEERING SPECIFICATION			CONTINUATION SHEET													
TITLE		DLVII-F ENGINEERING SPECIFICATION														
Bit	Name	Meaning and Operation														
10-9	RESERVED	Read only bit; cleared by INIT.														
7	RCVR DONE (Receiver Done)	Not applicable. Read as #s.														
		Thin bit is set when an entire character has been received and is ready for transfer to the LSI-11 Bus. When set, initiates an interrupt sequence provided RCVR INT END (bit 6) is also set.														
6	RCVR INT END (Receiver Interrupt Enable)	Cleared whenever the receiver buffer (RDUF1) is addressed or whenever RDR END (bit 0) is set.														
		Read only bit. Cleared by INIT.														
5-1	RESERVED	When set, allows an interrupt sequence to start when RCVR DONE (bit 7) sets.														
0	RDR END (Reader Enable)	Read/write bits cleared by INIT.														
		Not applicable. Read as #s.														
7.1.2	<u>Receiver Buffer Register</u>															
	[ERRORTC TFF TS] [RESERVED] [TPIPIPIPIPI]															
	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0															
FIGURE 3 RECEIVER BUFFER REGISTER (RBUT) - BIT ASSIGNMENTS																
Bit	Name	Meaning and Operation														
15	ERROR	Used to indicate that an error condition is present. Thin bit in the logical OR														
		[SIZE CODE NUMBER] A .. N.Y. F.F. G.C. REV														
FIGURE 4 TRANSMITTER STATUS REGISTER (XCSR) - BIT ASSIGNMENTS																
	[PROGRAMMABLE RATE] [TRANSMITTER] [MAINTENANCE] [BREAK] [BAUD RATE] [IEMS/SERVED] [RDY INT] [ISERVED] [ISERVED] [ ]															
	[SELECT] [LEN] [LEN] [LEN] [LEN] [LEN] [LEN] 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0															
FIGURE 4 TRANSMITTER STATUS REGISTER (XCSR) - BIT ASSIGNMENTS																
Bit	Name	Meaning and Operation														
15-12	PDR SEL (Programmable Baud Rate Select)	When set, these bits choose a baud rate from 50 - 19200 baud. See TABLE 1.														
		Write only bits; read as #s. Not cleared by INIT.														
11	PBR END (Programmable Baud Rate Enable)	This bit must be set in order to select a new baud rate indicated by bits 12 to 15.														
		Write only bit; read as #s. Not a latched bit.														
10-8	RESERVED	Not applicable, read as #s.														
7	XMIT RDY (Transmitter Ready)	This bit is set when the transmitter buffer (XDUF1) can accept another character. When set, it initiates an interrupt sequence provided XMIT INT END (bit 6) is also set.														
		Ready only bit. Set by INIT. Cleared by loading the transmitter buffer.														
6	XMIT INT END (Transmitter Interrupt Enable)	When set, allows an interrupt sequence to start when XMIT RDY (bit 7), is set.														
		Read/write bits cleared by INIT.														
5-3	RESERVED	Not applicable. Read as #s.														
2	MAINT (Maintenance)	Used for maintenance function. When set, connects the transmitter serial output to the receiver serial input while disconnecting the external device from the receiver serial input. It also forces the receiver to run at transmitter baud rate speed.														
		Read/write bit cleared by INIT.														
		[SIZE CODE NUMBER] A .. N.Y. F.F. G.C. REV														



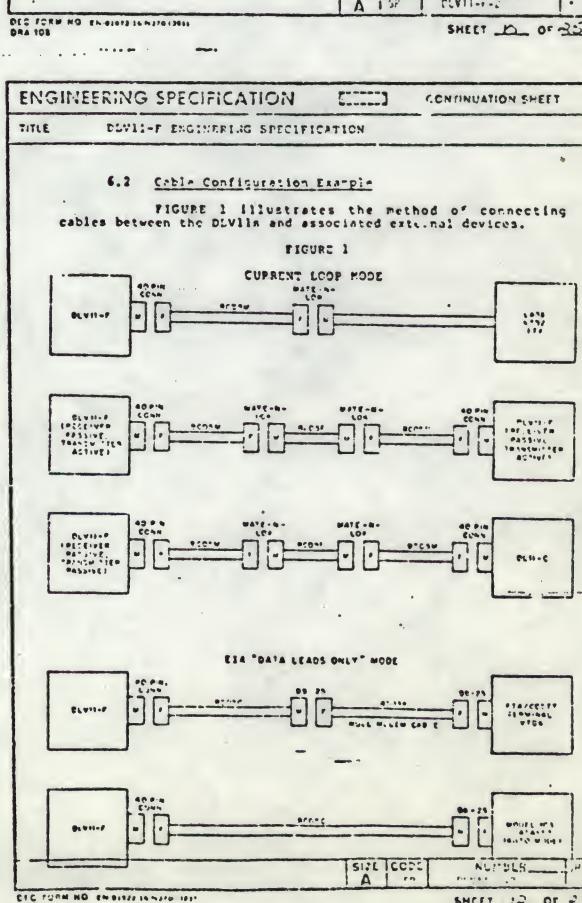
ENGINEERING SPECIFICATION		CONTINUATION SHEET																
TITLE DLV11-F ENGINEERING SPECIFICATION																		
6.0 CONFIGURATIONS																		
6.1 Jumper Definitions																		
<b>Jumper Definition</b>																		
A3-A12	Jumpers inserted will provide a patch with the corresponding bus Address bit. Selectable from 16000x to 17777x.																	
V3-VP	Jumpers inserted will assert the corresponding Vector address bit on the LSI-11 bus. Selectable from 00x to 77x.																	
RP-R3	UART receiver and transmitter baud rate select jumpers during common mode operation.																	
UART Receiver only baud rate select jumpers during split speed. See Table 1.																		
TP-T3	UART transmitter baud rate select jumpers during split speed operation and when the Maintenance Bit is set. (See Table 1.)																	
DG	Jumper inserted to enable frame generation.																	
P	Jumper inserted for parity generation by the UART. (Odd or even parity is selected by the -E jumper.)																	
-E	Jumper removed for Even parity and inserted for odd parity. (Receiver checks for appropriate parity and transmitter inserts the appropriate parity.)																	
6.2 Selects desired number of data bits. (I = Inserted, R = Removed.)																		
<table border="1"> <thead> <tr> <th></th> <th></th> <th>No. of Data Bits</th> </tr> </thead> <tbody> <tr> <td>I</td> <td>I</td> <td>5</td> </tr> <tr> <td>I</td> <td>R</td> <td>6</td> </tr> <tr> <td>R</td> <td>I</td> <td>7</td> </tr> <tr> <td>R</td> <td>R</td> <td>8</td> </tr> </tbody> </table>						No. of Data Bits	I	I	5	I	R	6	R	I	7	R	R	8
		No. of Data Bits																
I	I	5																
I	R	6																
R	I	7																
R	R	8																
C, CI																		
Jumpers inserted for common speed operation on UART receiver and transmitter clocks. (Note that jumpers S and SI must be removed.)																		
S, SI																		
Jumpers inserted for split speed operation on UART receiver and transmitter clocks. (Note that jumpers C and CI must be removed.)																		
SIZE CODE NUMBER REV A / P V111-F 1 OF 25																		

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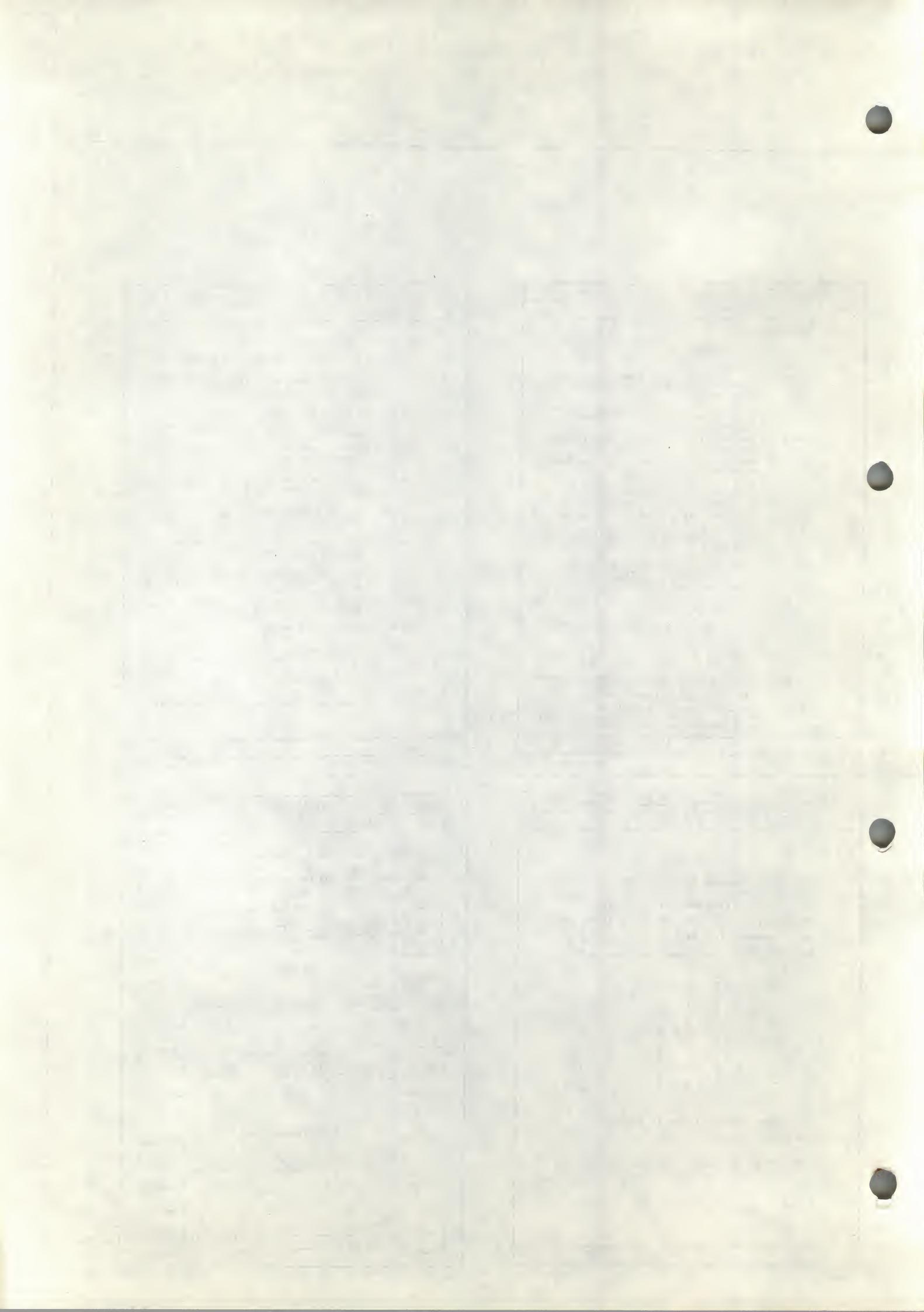
ENGINEERING SPECIFICATION		CONTINUATION SHEET			
TITLE DLV11-F ENGINEERING SPECIFICATION					
TABLE 1					
UART BAUD RATE SELECTIONS					
bit	bit	bit	bit		
Program Control (TCSR)	15	14	13	12	11 (See Note 1)
Receive Jumpers	R3	R2	R1	R0	Baud Rate
Transmit Jumpers	T3	T2	T1	T0	
I	I	I	I	I	50
I	I	I	R	R	75
I	I	R	I	R	110
I	I	R	R	I	134.5
I	I	R	I	I	150
I	I	R	I	R	300
I	I	R	R	I	600
I	I	R	R	R	1200
I	I	R	I	I	1800
I	I	R	I	R	2400
I	I	R	R	I	3600
I	I	R	I	R	4800
I	I	R	I	I	7200
I	I	R	R	I	9600
I	I	R	I	R	19200 (See Note 2)
I = Jumper Inserted = Program Bit Cleared					
R = Jumper Removed = Program Bit Set					
NOTE 1: Bit 11 of the TCSR (Write Only Bit) must also be set in order to select a non-Even Rate under program control. Also, jumper RD must be inserted to enable Baud Rate selection under program control.					
NOTE 2: At 19.2K baud, actual clock frequency is 316.8 KHz (3.145% error).					
SIZE CODE NUMBER REV A / P V111-F 11 OF 25					

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ENGINEERING SPECIFICATION		CONTINUATION SHEET	
TITLE DLV11-F ENGINEERING SPECIFICATION			
6.2 Jumper Definitions			
PD	Jumper inserted to enable programmable baud rate.		
H	Jumper inserted will assert the B HALT L on all received Framing Errors except when Maintenance Bit is set.		
B, -B	B Jumper inserted to assert B DCOK L on all received Framing Errors except when the Maintenance Bit is set. (-B Jumper must be removed.)		
2A, 2A, 3A	Jumpers inserted make the 2mA Current Loop receiver active. (Jumpers 1P and 2P must be removed.)		
1P, 2P	Jumpers inserted make the 2mA Current Loop receiver passive. (Jumpers 1A, 2A and 3A must be removed.)		
4A, 5A	Jumpers inserted make the 2mA Current Loop transmitter active. (Jumpers 3P and 4P must be removed.)		
3P, 4P	Jumpers inserted make the 2mA Current Loop transmitter passive. (Jumpers 4A and 5A must be removed.)		
-EP	Jumper removed enables the UNIT Frame Flags to be read in the high byte of the receiver Buffer.		
M	Jumper inserted to enable operation of the Maintenance bit (TCSK bit 2).		
M, MI	Manufacturing use only.		
NOTES: Jumpers are labelled to indicate whether they are inserted or removed to enable their corresponding features.			
(- marking) = Jumper inserted to enable feature.			
(--) marking = Jumper removed to enable feature.			
SIZE CODE NUMBER REV A / P V111-F 12 OF 25			



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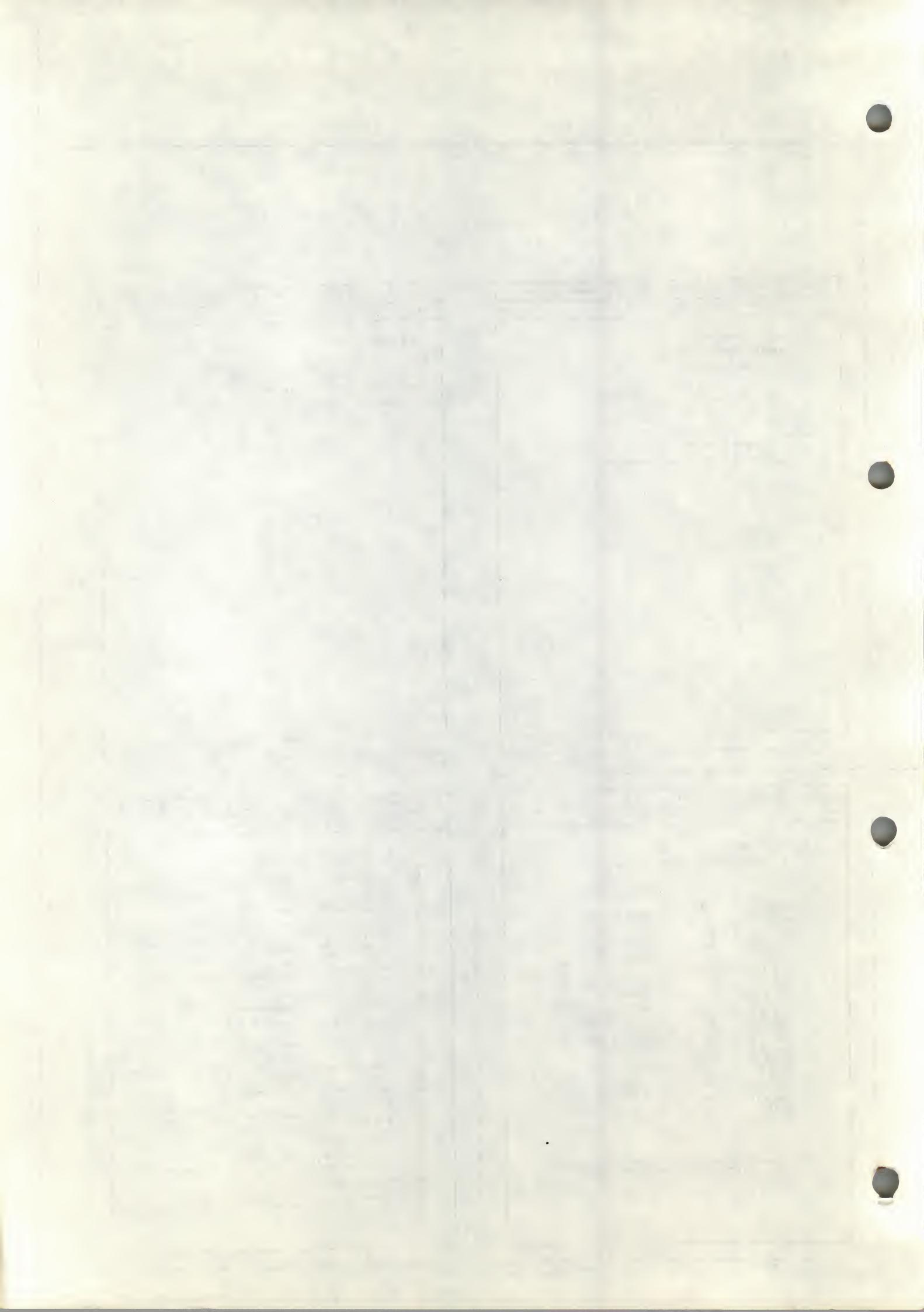


ENGINEERING SPECIFICATION				CONTINUATION SHEET			
TITLE DIV711-F ENGINEERING SPECIFICATION							
3.0 APPLICABLE DOCUMENTS							
EIA Standard (RS-232-C)							
D-CS-M8017							
A-ES-2913040 (DC005)							
A-PS-1912729 (DC004)							
A-PS-1912730 (DC003)							
A-PS-2112623 (SO16)							
DEC Std. 360 (LSI-11 Bus Specification)							
DEC Std. 102 (Computer Environment Std.)							
SHEET	5	OF	25				

ENGINEERING SPECIFICATION				CONTINUATION SHEET			
TITLE DIV711-F ENGINEERING SPECIFICATION							
5.0 EXTERNAL CONNECTIONS							
5.1 DIV711-F Edge Connector Pinning							
45	AA2	BIRD 1	AL2				
42	AD2	BRPLY 1	AF2				
BDT	AP2						
BDAL 1 L	AU2						
BDAL 1 P L	AV2	BSYNC 1	AJ2				
BDAL 2 L	EE2						
BDAL 3 L	RF2	GND	AC2				
BDAL 4 L	DH2	GND	AT1				
BDAL 5 L	DJ2						
BDAL 6 L	BK2						
BDAL 7 L	PL2	GND	BC2				
BDAL 8 L	DM2	BDCOK N	BA1				
FRAL 9 L	RH2						
FRAL 10 L	RF2	GND	BT1				
BDAL 11 L	DR2	MSPAR: A -12V	AK1				
BDAL 12 L	SC2	MSPAR: A -12V	AL1				
BDAL 13 L	BT2	MSPAR: B	BK1				
BDAL 14 L	DU2	MSPAR: B (EXT R CLK)	BL1				
BDAL 15 L	BV2						
BDIN L	AH2						
BDOUT L	AE2						
BHALT L	AP1						
PIAK 1 L*	AM2	SEPAR 3 (EXT T CLK)	BH1				
PIAK 0 L*	AN2						
BDINIT L	AT2						
BDGNDL*	AR2						
BDGNDL*	AS2						
* These signal pairs are not bussed but pins through this module in order to propagate the delay chain.							
SHEET	5	OF	25				

ENGINEERING SPECIFICATION				CONTINUATION SHEET																											
TITLE DIV711-F ENGINEERING SPECIFICATION																															
4.0 POWER REQUIREMENTS																															
<table border="1"> <thead> <tr> <th></th> <th>TYP</th> <th>AMP</th> <th>TYP</th> <th>WATT</th> <th>TYP</th> <th>AMP</th> <th>WATT</th> </tr> </thead> <tbody> <tr> <td>+5 Volt ± 5%</td> <td>1.0</td> <td>Amps</td> <td>1.5</td> <td>Amps</td> <td>SW</td> <td>7.5W</td> <td></td> </tr> <tr> <td>+12 Volt ± 3%</td> <td>150mA</td> <td></td> <td>230mA</td> <td></td> <td>SW</td> <td>2.8W</td> <td></td> </tr> </tbody> </table>									TYP	AMP	TYP	WATT	TYP	AMP	WATT	+5 Volt ± 5%	1.0	Amps	1.5	Amps	SW	7.5W		+12 Volt ± 3%	150mA		230mA		SW	2.8W	
	TYP	AMP	TYP	WATT	TYP	AMP	WATT																								
+5 Volt ± 5%	1.0	Amps	1.5	Amps	SW	7.5W																									
+12 Volt ± 3%	150mA		230mA		SW	2.8W																									
SHEET	6	OF	25																												

ENGINEERING SPECIFICATION				CONTINUATION SHEET			
TITLE DIV711-F ENGINEERING SPECIFICATION							
5.2 40-Pin Connector Pinning							
Header	Pin	M8028 Module	BC01V Modem Cable	BC05W 20mA Cable			
A		Ground		Ground			
B		Ground					
C		Force Busy(EIA)	Force Busy				
D							
E		Serial Input(TTL)	Interlock In <---	Interlock In			
F		Serial Output(EIA)	Transmitted Data				
G		20mA Interlock					
H		Serial Input (EIA)	Received Data	Interlock Out			
I		Serial Input(20mA)					
J		External Clock		Received Data			
K		Interlock Out ---					
L		Serial Clock Xmt					
M							
N		Serial Clock Revr					
O		Serial Input-(20mA)					
P		Clear to Send	Received Data				
Q		Request to Send					
R		(EIA)					
S							
T							
U							
V							
W							
X							
Y							
Z							
AA		Serial Output+(20mA)	Data Set Ready	Transmitted Data			
BB			Carrier				
CC		Clock Input (TTL)	Data Terminal Rdy				
DD		Data Terminal Pdy	(EIA)				
EE		Reader Run-(20mA)					
FF							
HH		Borg Clock Enb	202 Sec Rmt	Reader Run			
JJ			202 Sec Revr				
KK							
LL		Serial Output-(20mA)		Transmitted Data			
MM							
PP		Reader Run+(20mA)					
RR							
SS		Serial Output(TTL)	-				
TT		+5V					
UU		Ground					
VV		Ground	Ground	Ground	Ground	Ground	Ground
SHEET	6	OF	25				

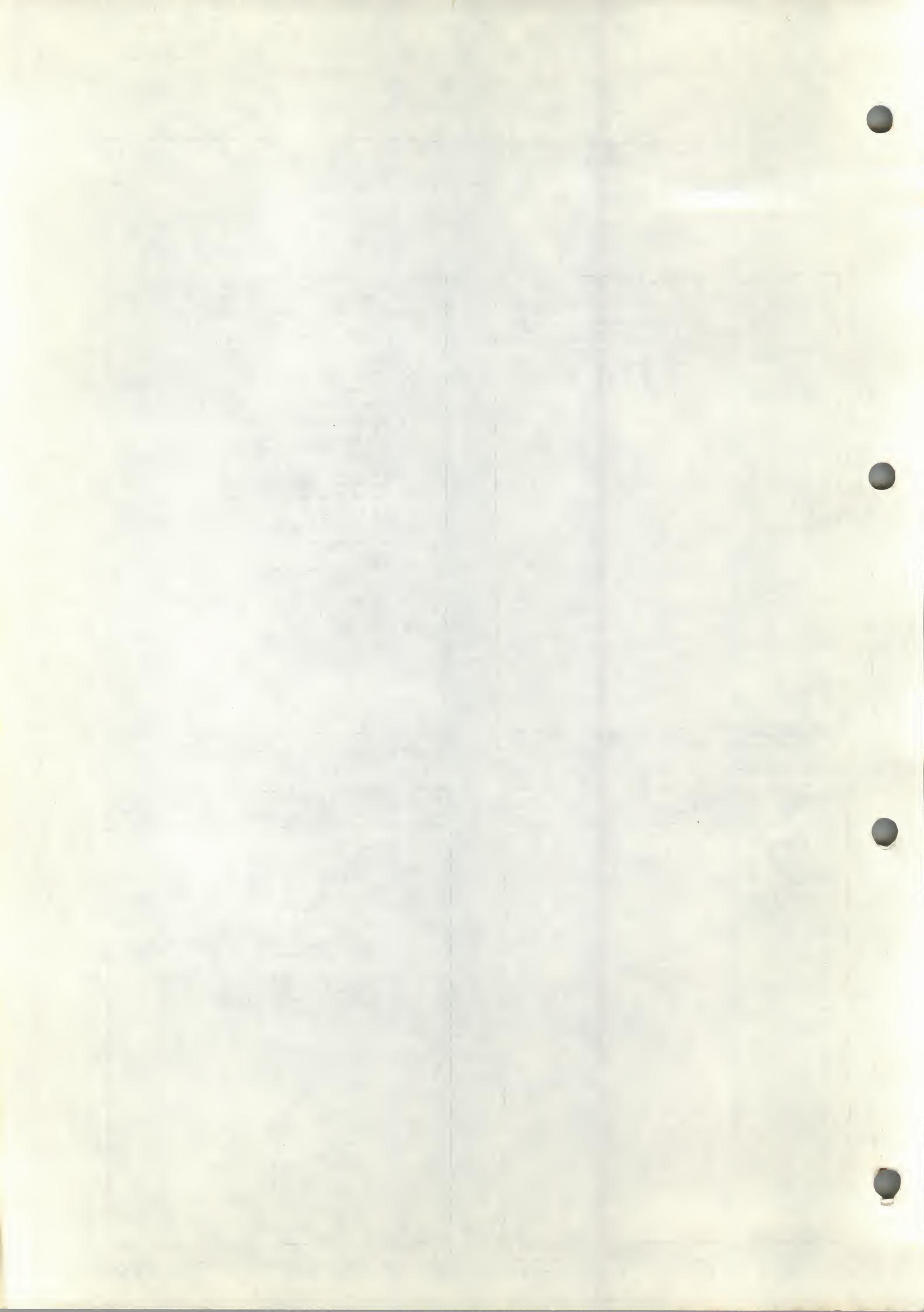


DIGITAL EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS					
ENGINEERING SPECIFICATION			DATE 6 MARCH 73		
TITLE	LEVEL ENGINEERING SPECIFICATION				
REV	DESCRIPTION	REVISIONS		APPROVED BY	DATE
		CHG NO	013		

ENGINEERING SPECIFICATION		CONTINUATION SHEET			
TITLE DLV11-F ENGINEERING SPECIFICATION					
TABLE OF CONTENTS					
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ENGINEERING SPECIFICATION		CONTINUATION SHEET	
TITLE	DEVI1-F ENGINEERING SPECIFICATION		
1.0 SCOPE			
<p>The scope of this document is to present the description and specification for the DEVI1-F (M5018) Asynchronous Line Interface. It describes the DEVI1-F both physically and functionally.</p>			
SIZE A	COPY	NUMBER DRAFT	PREV

ENGINEERING SPECIFICATION				CONTINUATION SHEET	
TITLE		DLVII-F ENGINEERING SPECIFICATION			
<b>2.0 GENERAL DESCRIPTION</b>					
<p>The DLVII-F is an interface between an asynchronous serial line and the LSI-11 Bus. The LSI-11 Bus circuitry is designed in accordance with DEC Std 150 "LSI-11 Bus Specification". All circuitry is housed on one dual extended height module (MDU2B) and mounts in any standard LSI-11 backplane. The DLVII-F supports the following two modes of operation:</p>					
<p><b>1. Current Loop Mode</b></p> <p>20mA current loop circuits are supplied to the external device via a female MATE-N-LOCK connector when used with the BC05M-XX cable.</p>					
<p><b>2. EIA "Data Leads Only" Mode</b></p> <p>EIA drivers and receivers are supplied to the external device via a male DB25 connector used with the BC04V-XX cable.</p>					
0 61					
SIZE A	CODE CP	NUMBER REV. 1.7.0			



### Kanalunabhängige Brücken

Brücke	Std.	Stellung	Std.	Anw.	Brücke	Bed.	Stellung	Std.	Anw.	Brücke	Bed.	Stellung	Std.	Anw.
A12	3	X-0	X-1	X	A6	J	R	C1	Konsol auf	X-0	X	X-1	X	
A11	1	X-0	X-1	X	A5	P	x-0	C2	CH3	X-0	X	X-1	X	
A10	4	X-0	X-1	X	V7	J	R	Break	Jnh.	R	X-H	X		
A9	5	X-0	X-1	X	V6	J	R	Reakt.	Halt	X-H	X	X-B		
A8	6	X-0	X-1	X	V5	J	x-0	CH3	Boott	X-B	.	.	.	
A7	7	R	J											

Std.-Adr. 177.500 Anw. - Adr. : Std.-Vec. : 300 Anw. - Vec. :

Einstellung je Kanal

Brücke	Bedeutung	Ø			1			2			3		
		Std.	Anw.	Stellung	Std.	Anw.	Stellung	Std.	Anw.	Stellung	Std.	Anw.	
D	7 Datenbits	bd	0-U	1-U	2-U			3-U					
	8 Datenbits	bd	0-T	1-T	2-T			3-T					
S	1 Stop Bit	bd	0-V	1-V	2-V			3-V					
	2 Stop Bits	kd	0-W	1-W	2-W			3-W					
P	2,4 kbd	kd	0-Y	1-Y	2-Y			3-Y					
	4,8 kbd	kd	0-L	1-L	2-L			3-L					
	9,6 kbd	kd	0-N	x	2-N	x		3-N	x				
E	19,2 kbd	kd	0-K	1-K	2-K			3-K					
	38,4 kbd	kd	0-Z	1-Z	2-Z			3-Z					

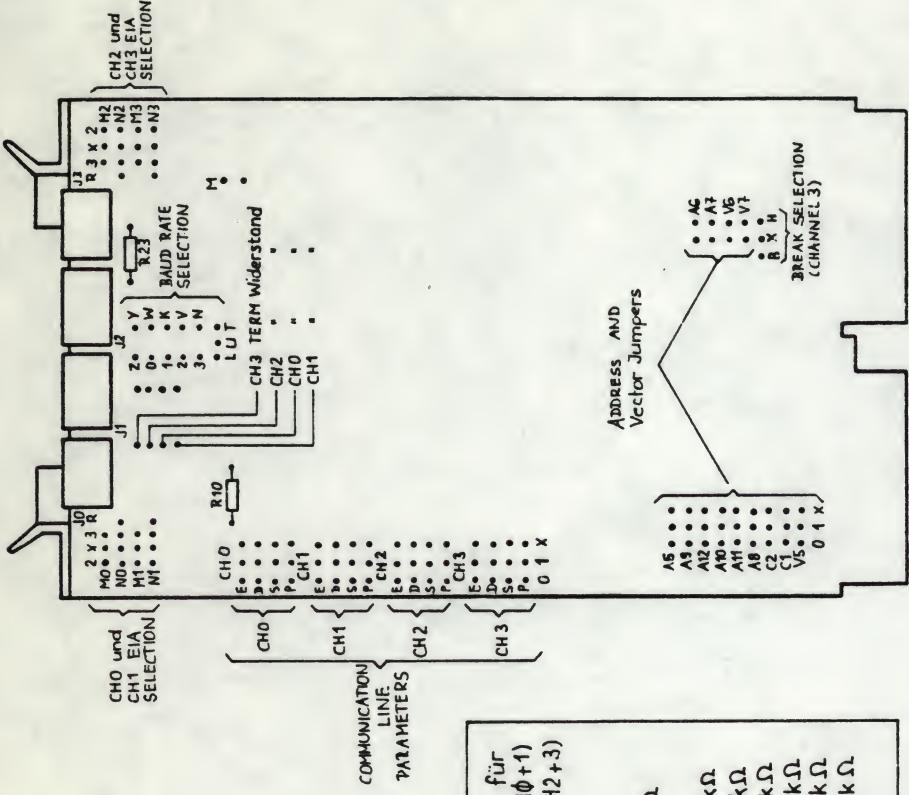
Tabelle für  
R10 (CHΦ+1)  
R23 (CH2+3)

150	bd	0-U	1-U	2-U	3-U	1MΩ
300	bd	0-T	1-T	2-T	3-T	
600	bd	0-V	1-V	2-V	3-V	
1,2	kd	0-W	1-W	2-W	3-W	
2,4	kd	0-Y	1-Y	2-Y	3-Y	
4,8	kd	0-L	1-L	2-L	3-L	
9,6	kd	0-N	x	2-N	3-N	
19,2	kd	0-K	1-K	2-K	3-K	
38,4	kd	0-Z	1-Z	2-Z	3-Z	

Standard: Bildschirm-Terminals (3-Koerse) Anwendung:

M+N	TERM	EIAR5422	X-2	X-2	X-2	X-0	X-0	X-1	X-1	X-0	X-0	X-1	X
M+N	V24	400Ω				100Ω							
M+N	20mA mit 900.641	X-3	X-3	X-3	X-R	X	X-3	X	X-3	X	X-3	X	
M+N		X-R	X	X-R	X								

R = entfernt  
J = eingesetzt



78	79	Name	Name
27.44	μA/ser	28.64	μA/ser
Caro		Caro	
Rivm		Rivm	

Standard: Einstell - Tabelle für DLV 11 - J (M 8043)

B 900.610.3

